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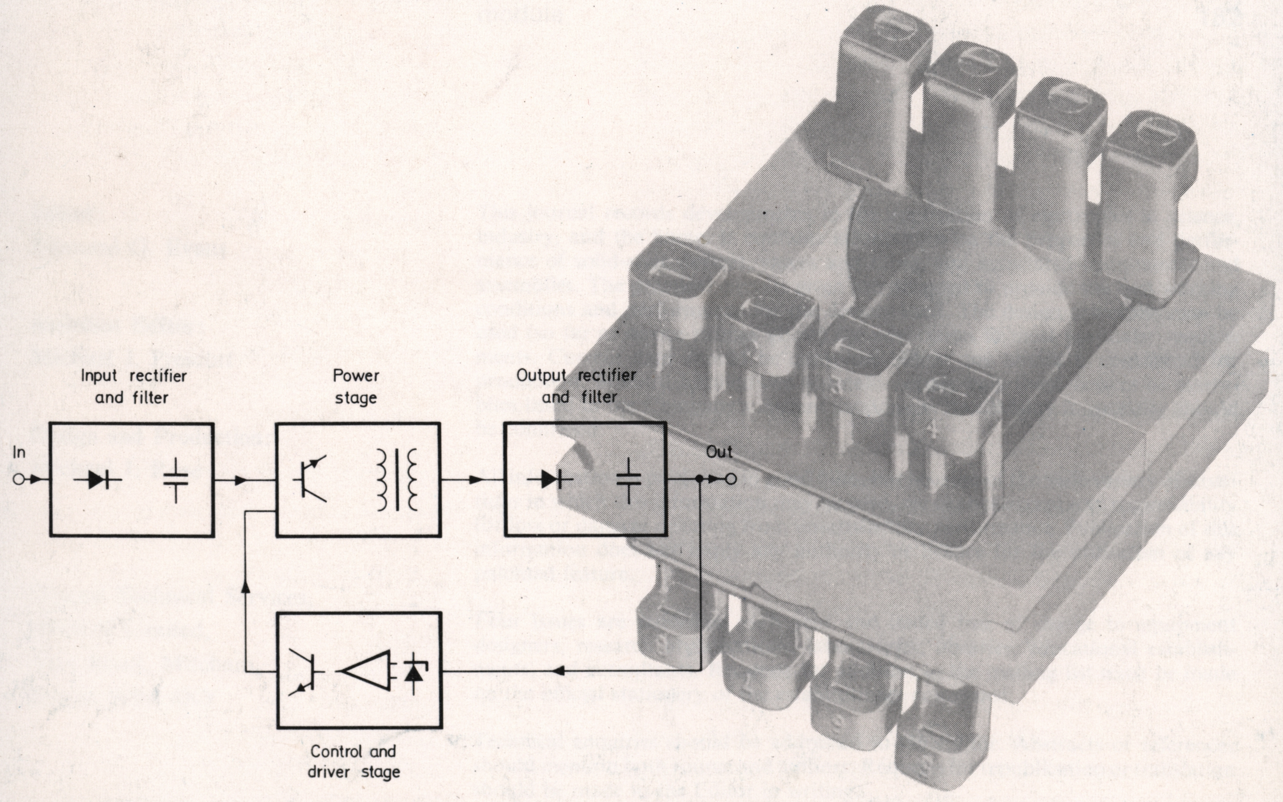
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- Base circuit design for high-voltage switching transistors in power converters
- Cores for switched-mode power supply transformers
- CL8960 X-band doppler radar module

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Cover Picture:
The simple block diagram of a switched-mode power supply is superimposed on a Mullard switched-mode power supply 500W transformer core pair, type FX3750, with bobbin.

The newly-styled Mullard Technical Communications cover will from now on carry a topical artwork each issue.

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This journal records developments in the application of electronics in science, industry, and the home. It contains information on the properties and performance of solid-state devices, valves and tubes, and associated components and assemblies. The practical circuits given are designed to provide the best working conditions and performance for the devices used. The design principles may be used (so far as device ratings allow) for adaptation to meet particular requirements. Current data should be consulted before any circuit is considered for production. Mullard Limited can normally supply only those devices or assemblies listed in the Company's current catalogues. Availability in quantity should be confirmed.

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Titanium-gold: high-reliability transistor metallisation

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The life expectancy of semiconductor devices can be substantially improved by substituting a titanium-gold metallisation for the aluminium metallisation commonly used in silicon semiconductor devices. An aluminium wire may work-harden due to stresses, whilst a gold wire has the tendency to form compounds with the aluminium, embrittling the joint.

Extensive accelerated life tests were carried out on batches of BFW16A, BFW30, and BFY90 transistors provided with titanium-gold metallisation. These tests revealed that neither breakdowns nor degradation of these semiconductor devices is to be expected within 10^6 hours (about 100 years) if they are operated at their specified ratings.

INTRODUCTION

The nature of the metallic film applied to the surface of a semiconductor chip to enable electrical contacts to be made is crucial to the performance of the device. In the past, films of aluminium have generally been used for this purpose, and this method has proved highly satisfactory for the great majority of hermetically encapsulated devices, giving long life and high reliability. However, with the recent increased use of plastic encapsulation, the limitations of the well-tried aluminium metallisation method have become apparent. Severe thermal stresses in the plastic can result in strain in the aluminium bonding wires and consequent possible mechanical failure. Gold bonding wires have greater mechanical strength, but if used directly to replace aluminium, gold-aluminium intermetallic compounds (purple plague) can result and lead again to possible contact failure. A further, if less important, problem associated with aluminium metallisation is that of electrolytic corrosion. Also, with the introduction of u.h.f. and microwave power devices operating at elevated temperatures and requiring complex, finely delineated contacting patterns, aluminium metallisation has proved inadequate because of the effects of electro-migration.

These problems have led therefore to the introduction of alternative metallisation techniques, in particular those employing gold as the contacting metal. Several gold metallisation systems have been developed, each applicable to particular devices and applications. In this article, one such gold metallisation system, employing titanium as a barrier metal, is described.

MOUNTING OF THE SEMICONDUCTOR CHIP

Although this article actually deals with far more complex transistors, it will be assumed for the sake of simplification that the chip of a silicon diode is mounted on a header. (In fact, such diodes are usually mounted in a different manner.)

Wherever it is necessary to make ohmic (that is, non-rectifying) connections to a semiconductor device, or connections between parts of an integrated circuit, the relevant surfaces of the chip must be coated with a layer of some good conductor. The conductor which is used for these contact points has several important requirements to satisfy: it must have low resistivity, adhere well to silicon and to any residual silicon dioxide, and must not react with silicon at any temperature at which subsequent processing is carried out. Such a conductor should also be easy to apply evenly, and easy to make further contact to. A conductor which satisfies most of these requirements is aluminium, which is at present commonly used in semiconductor device fabrication.

The investigations on which this article is based were made by A. Verbokken and W. Leenders of the Philips' Semiconductor Quality Laboratory, Nijmegen, The Netherlands; the information on metallisation technology was supplied by B. Symersky of the Philips' Semiconductor Development Laboratory, also at Nijmegen.

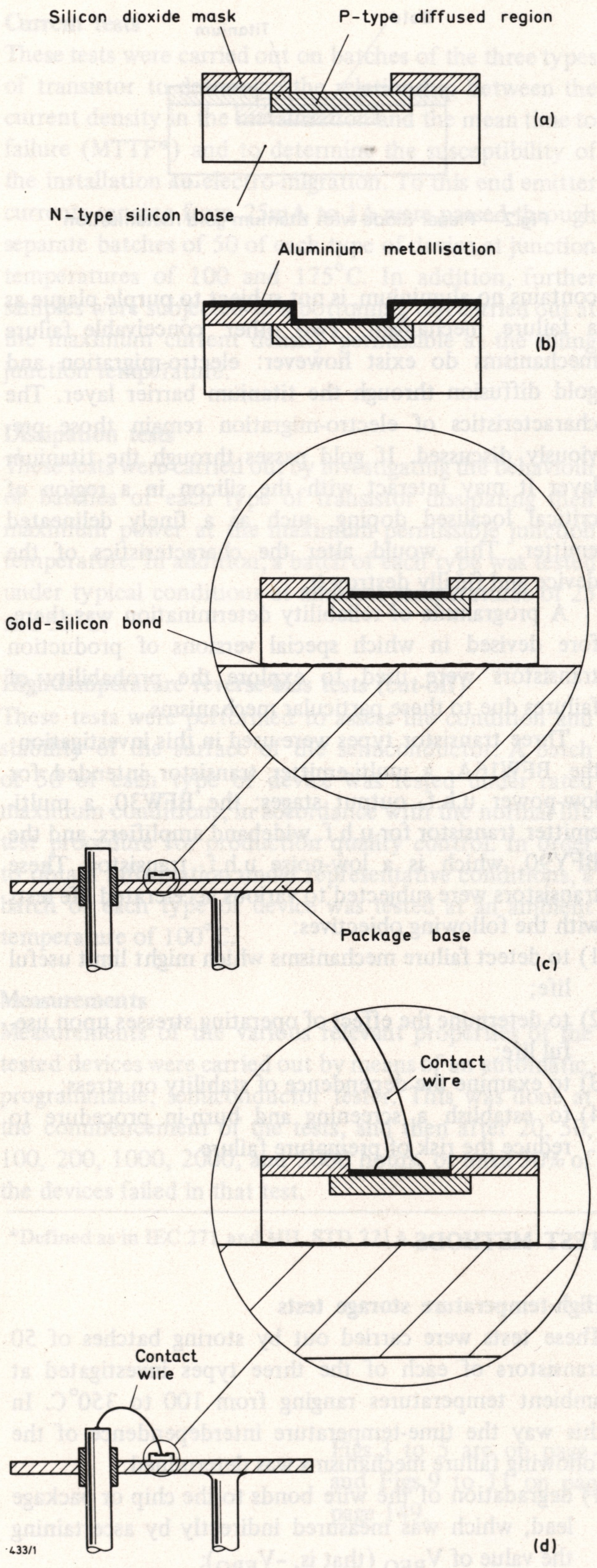

Fig.1 — Stages in connecting semiconductor chip to package:
a) simple chip containing planar diode
b) aluminium metallisation
c) chip bonded to package base by means of gold-silicon eutectic
d) lead connects chip to package

The various customary stages in making a connection from a semiconductor device to a package lead are illustrated by Fig.1. The device itself is a planar-processed diode. One electrode is exposed through a gap in the silicon dioxide layer, through which p-type impurities have been diffused to form the junction; the other electrode is the n-type base. The chip before metallisation appears as in Fig.1a.

The chip is coated with aluminium, Fig.1b, by sublimation in a vacuum, and the surplus aluminium removed. Next, the chip is bonded to the gold-plated header (or lead), Fig.1c, by a gold-silicon eutectic solder pellet at a temperature above 370°C. This chip bonding temperature imposes the first limiting requirement upon the metallisation: it must not react with silicon at or below this temperature.

After having been bonded to the header, the chip is ready to receive the final connection. This is in the form of a thin metal wire, which is bonded to both the metallic coating of the chip and the package lead, Fig.1d. The finished component is now ready for encapsulation.

An important step in the construction of a packaged device is the selection of a suitable material for the wire connecting the chip to the package lead. This wire should be easy to bond to aluminium and should form a strong, stable joint. Both gold and aluminium wires bond readily to a clean aluminium film, gold being the easier of the two to bond mechanically. Aluminium suffers from the disadvantage that it is rather brittle when work-hardened, and work-hardening can be caused by the thermal mismatch between the wire and the plastic encapsulation. For these reasons, gold leads are preferred, the extra cost being very small as the wires used are of small dimensions.

FAILURES

The major cause of semiconductor components breaking down when operated within their ratings proves to be contact failure. Apart from mechanical stresses, the three following principal failure mechanisms are to be distinguished in devices constructed as outlined above.

Purple plague and black death

These are terms used to describe the results of the Kirkendall effect, the formation of intermetallic compounds of gold and aluminium which occurs at elevated temperatures. It is believed that, during the formation of these compounds, aluminium diffuses into gold faster than gold into aluminium. Voids and cracks form, weakening the already brittle intermetallic joint, until any small stress can cause the joint to fracture.

Corrosion
Aluminium is particularly susceptible to electrolytic corrosion. In hermetically-sealed packages this is not a problem, but in plastic encapsulations corrosion can severely limit the life of a device at high junction temperatures.

Electro-migration
This occurs in metal films carrying current at a density of the order of $2 \times 10^3\,A/mm^2$ as encountered in semiconductor practice. Electro-migration may be likened to a 'wind' effect; the high-speed high-density electron flow 'sweeps' conductor material from the grain boundary regions of a film. This causes material distribution to become uneven and, because of the resulting void formation, leading to still higher current densities, the process may become catastrophic.

THE TITANIUM-GOLD SYSTEM

With the object of finding a cure for the above failure mechanisms, thorough investigations were undertaken with alternative types of metallisation. The results obtained with the titanium-gold system were very encouraging.

The particular metallisation system which is adopted for any given device type is determined to a large degree by the geometry necessary to achieve the required characteristics of that component. It is not the intention here to discuss the influence of device geometry on metallisation, although several systems have been developed and proved, each with its own area of application.

The titanium-gold metallisation system described here has been specially developed for very high frequency telecommunications devices, where long life at high temperatures is required. The system was arrived at by considering each of the problem areas and their individual solutions, and combining these solutions into a practical high-reliability method.

In many ways, gold is an ideal metal for coating semiconductors. It has excellent corrosion resistance, and is far less susceptible to electro-migration than aluminium; moreover, it is easy to deposit. Unfortunately, gold should not be deposited directly on to silicon because it will form an alloy at the bonding temperature, and it does not adhere well to silicon dioxide. Some barrier layer is therefore required between the silicon and the gold. The metal chosen for this application was titanium. This metal is easy to deposit, does not react readily with either silicon or gold, adheres well to silicon dioxide, and does not easily corrode. The final device contact, as used with the simple component of Fig.1, is similar to the arrangement shown in Fig.2.

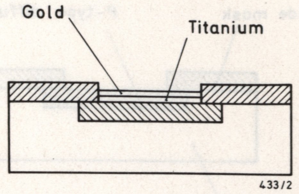

Fig.2 — Planar diode with titanium-gold metallisation

The titanium-gold metallisation system, because it contains no aluminium, is not subject to purple plague as a failure mechanism. Two other conceivable failure mechanisms do exist however: electro-migration and gold diffusion through the titanium barrier layer. The characteristics of electro-migration remain those previously discussed. If gold passes through the titanium layer it may interact with the silicon in a region of critical localised doping, such as a finely delineated emitter. This would alter the characteristics of the device and finally destroy it.

A programme of reliability determination was therefore devised in which special versions of production transistors were used to explore the probability of failures due to these particular mechanisms.

Three transistor types were used in this investigation: the BFW16A, a multi-emitter transistor intended for low-power u.h.f. output stages; the BFW30, a multi-emitter transistor for u.h.f. wideband amplifiers; and the BFY90, which is a low-noise u.h.f. transistor. These transistors were subjected to various accelerated life tests with the following objectives:

1) to detect failure mechanisms which might limit useful life;
2) to determine the effect of operating stresses upon useful life;
3) to examine the dependence of stability on stress;
4) to establish a screening and burn-in procedure to reduce the risk of premature failure.

TEST METHODS

High-temperature storage tests
These tests were carried out by storing batches of 50 transistors of each of the three types investigated at ambient temperatures ranging from 100 to 350°C. In this way the time-temperature interdependence of the following failure mechanisms was determined:

1) degradation of the wire bonds to the chip or package lead, which was measured indirectly by ascertaining the value of V_{BEO} (that is, $-V_{EBO}$);
2) degradation of the chip-to-header bond, which was measured indirectly by ascertaining the values of V_{BCO} (that is, $-V_{CBO}$) and $V_{CE(sat)}$;
3) degradation of the parameters h_{FE} and $V_{(BR)EBO}$ caused by the diffusion of gold through the titanium barrier layer.

Current tests
These tests were carried out on batches of the three types of transistor to determine the relationship between the current density in the metallisation and the mean time to failure (MTTF*) and to determine the susceptibility of the installation to electro-migration. To this end emitter currents ranging from 25mA to 1A were passed through separate batches of 50 of each type of device at junction temperatures of 100 and 175°C. In addition, further samples were subjected to a bottoming test carried out at the maximum current density permissible at the ruling junction temperature.

Dissipation tests
These tests were carried out by investigating the behaviour of batches of each type of transistor dissipating their maximum power at the maximum permissible junction temperature. In addition, a batch of each type was tested under typical conditions at ambient temperatures of 25 and 55°C.

High-temperature reverse-bias tests (cut-off)
These tests were performed to assess the condition and stability of the surface of the semiconductor. A batch of 50 of each type of device was tested under rated maximum conditions, in accordance with the normal life test procedure for production quality control. In order to obtain information under representative conditions, a batch of each type of device was tested at an ambient temperature of 100°C.

Measurements
Measurements of the various relevant properties of the tested devices were carried out by means of an automatic, programmable, semiconductor tester. This was done at the commencement of the tests, and then after 20, 50, 100, 200, 1000, 2000, and 5000 hours, or until 50% of the devices failed in that test.

GRAPHICAL REPRESENTATION OF THE TESTS

The results obtained from the foregoing tests were analysed by standard methods, with the aid of a computer program developed for this purpose. Mathematical models of the three types of device used in the evaluation programme, with separate models for stability and complete failures, were constructed to improve the analyses.

The terms used to describe the quality and reliability of the devices under consideration are taken from the IEC publication No.271 (1969).

To investigate the influence of the storage temperature on the leakage current I_{BEO}, batches of the three transistors with titanium-gold metallisation were stored at various temperatures up to 350°C. The time at which I_{BEO} had reached 10nA at an ambient temperature of $T_{amb} = 25°C$ was taken as the failure criterion of the devices. The cumulative percentage of failures was plotted on a Weibull probability chart, and from this chart the times were found at which 10, 50, and 90% of the devices fail. These times were then plotted as a function of temperature. Figs.3, 4, and 5 compare results obtained for the three device types.

Similar tests were carried out to investigate the deterioration of h_{FE} by taking as the failure criterion the time at which the required base current variation ΔI_B at a specified adjustment had reached an increase of 50%. Figs.6, 7, and 8 show the results obtained.

To investigate the occurrence of gold diffusion through the titanium barrier layer, the information obtained from the Weibull chart was plotted on an Arrhenius graph, with the reciprocal of temperature (×1000) as the ordinate and log-time as the abscissa. A number of charts thus obtained for the three types of transistor are shown in Figs.9, 10, and 11. By combining these charts for all devices under test, Fig.12 was obtained.

Finally, Fig.13 shows a plot of life expectancy, for all the devices, as a function of current density, the occurrence of open-circuits or short-circuits due to electro-migration being taken as the failure criterion.

text contd. on p.149.

Figs.3 to 5 are on page 146, Figs.6 to 8 on page 147, and Figs.9 to 11 on page 148. Figs.12 and 13 are on page 149.

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*Defined as in IEC 271 and MIL STD 721A.

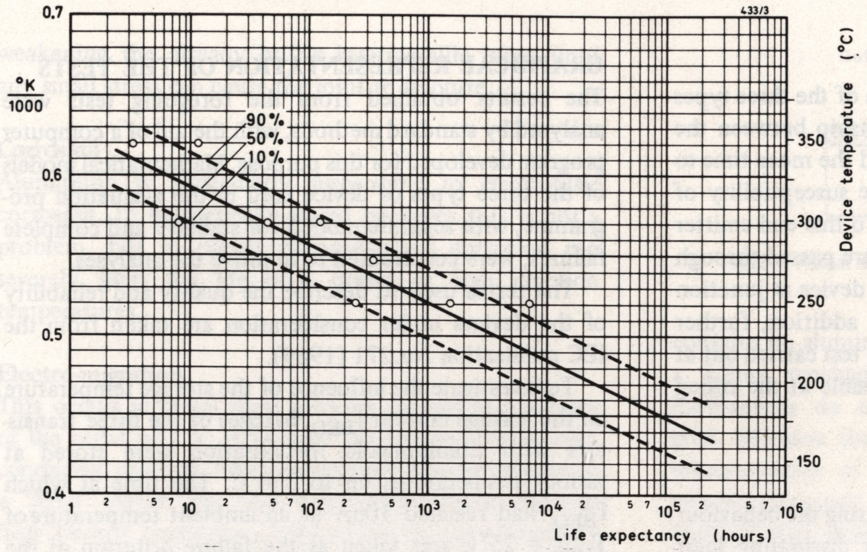


Fig.3 – BFW16A: 10%, 50%, and 90% percentiles for the failure criterion $I_{EBO} \geq 10nA$ at $T_{amb} = 25°C$, $V_{CE} = 1V$

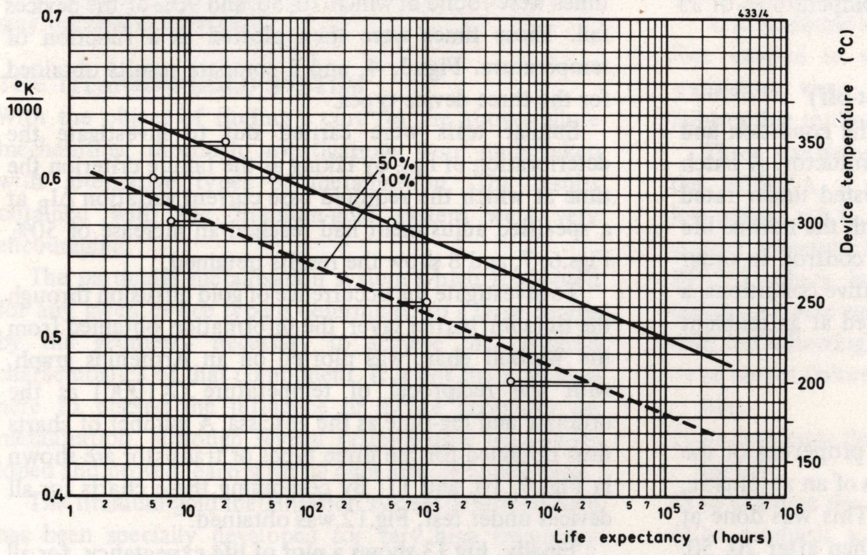


Fig.4 – BFW30: 50% and 10% percentiles for the failure criterion $I_{EBO} \geq 10nA$ at $T_{amb} = 25°C$, $V_{CE} = 1.5V$

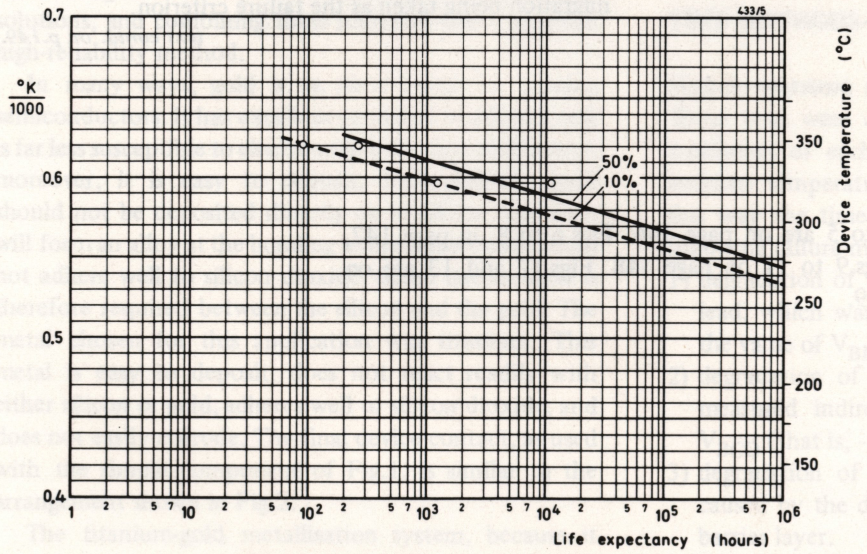


Fig.5 – As Fig.4, but for the BFY90

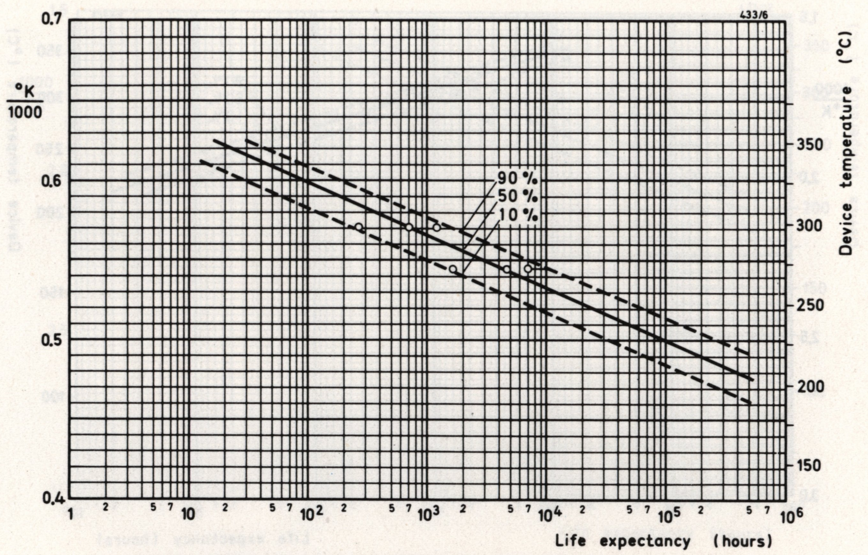


Fig.6 – BFW16A: 10%, 50%, and 90% percentiles for the failure criterion $\Delta I_B \geq 50\%$ at $I_C = 50mA$, $V_{CE} = 5V$

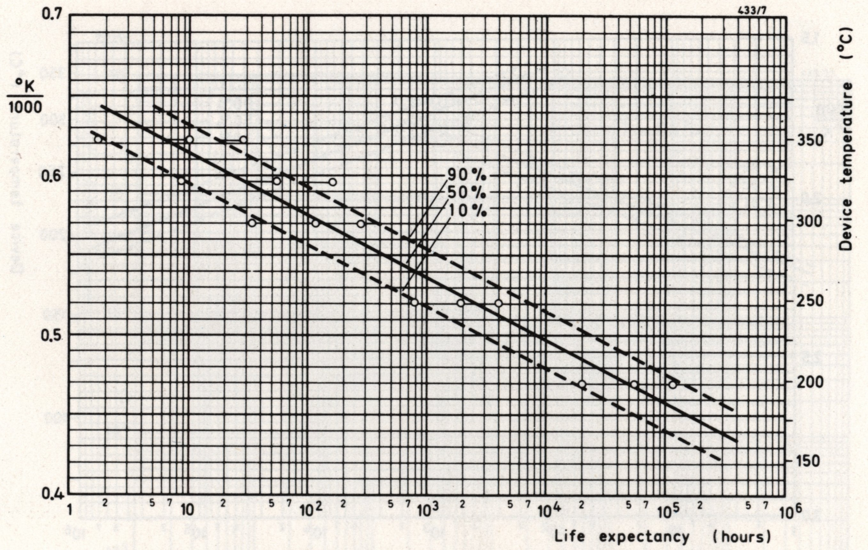


Fig.7 – BFW30: 10%, 50%, and 90% percentiles for the failure criterion $\Delta I_B \geq 50\%$ at $I_C = 20mA$, $V_{CE} = 5V$

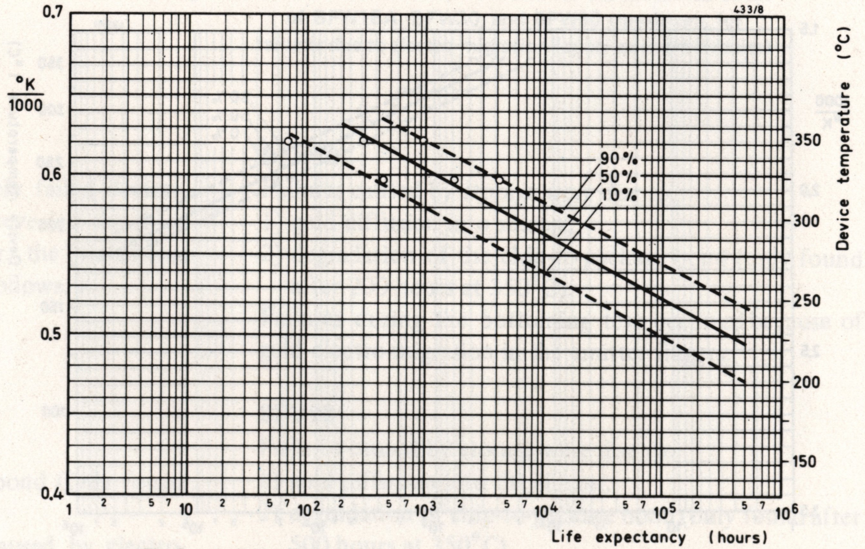


Fig.8 – BFY90: 10%, 50%, and 90% percentiles for the failure criterion $\Delta I_B \geq 50\%$ at $I_C = 2mA$, $V_{CE} = 5V$

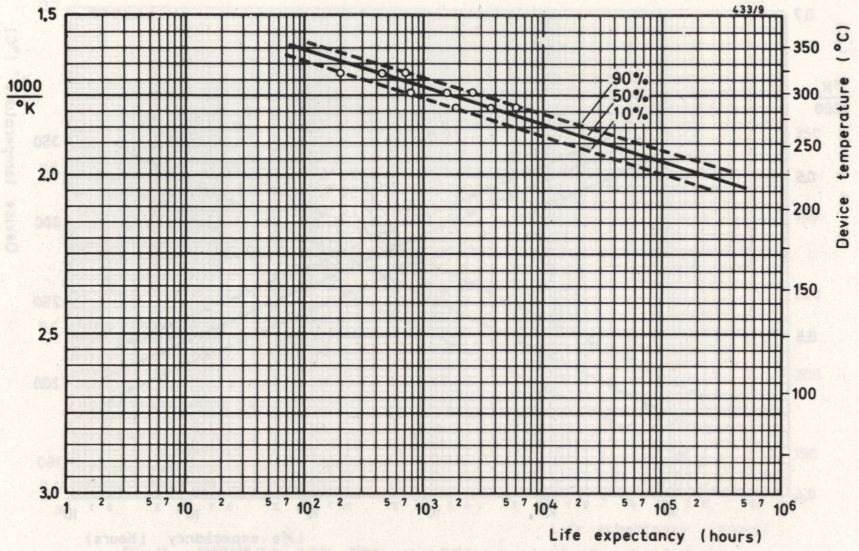


Fig.9 – BFW16A: 10%, 50%, and 90% percentiles for failures due to migration of gold through the titanium barrier layer

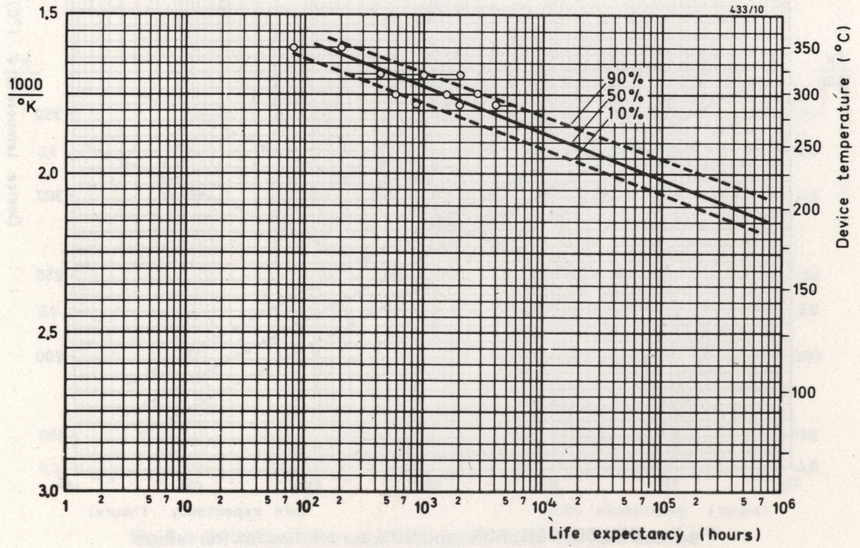


Fig.10 – As Fig.9, but for the BFW30

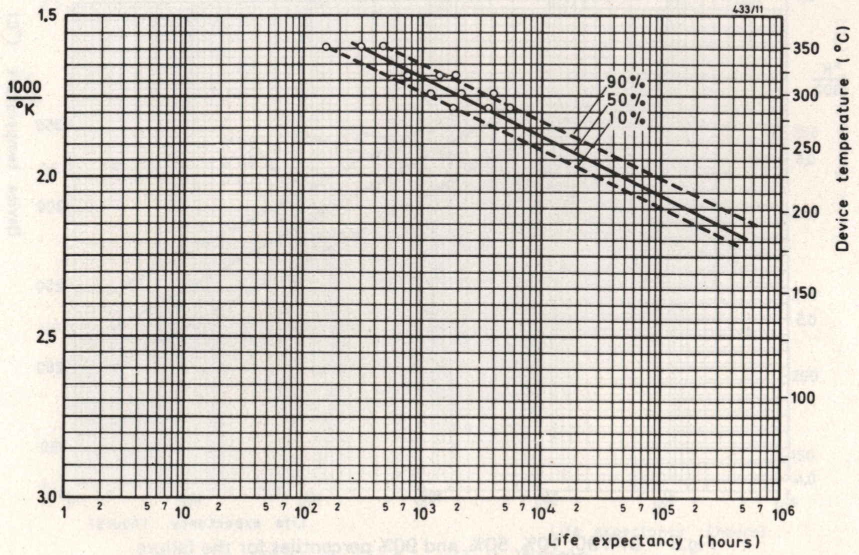


Fig.11 – As Fig.9, but for the BFY90

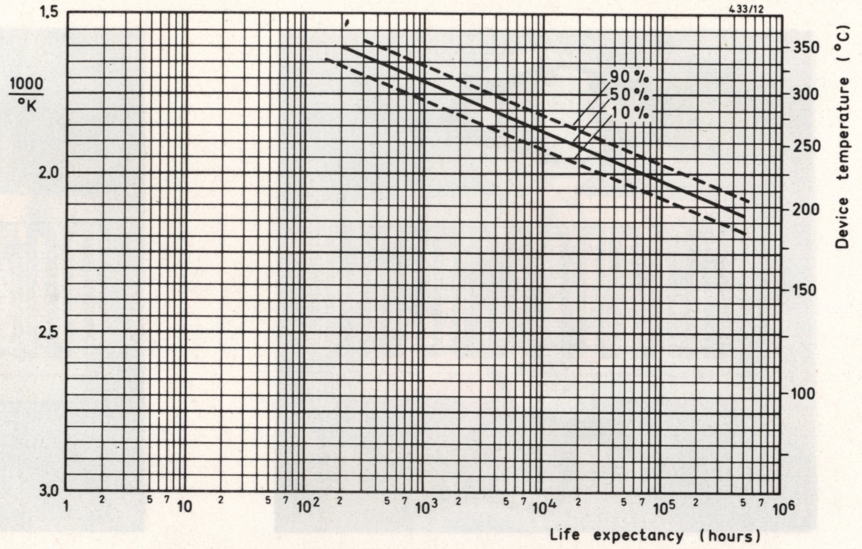


Fig.12 – 10%, 50%, and 90% percentiles for the combined batch of BFW16A, BFW30, and BFY90 transistors, for failures due to migration of gold through the titanium barrier layer

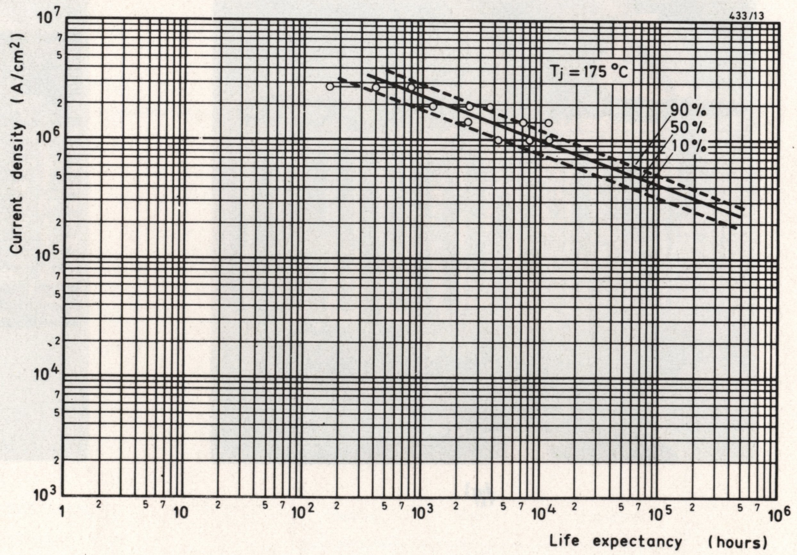


Fig.13 – 10%, 50%, and 90% percentiles for the combined batch of BFW16A, BFW30, and BFW90 transistors, for failures due to electro-migration (open- or short-circuits)

ANALYSIS OF THE FAILURES

Microscopic examination of completely failed devices, some of which are shown in Fig.14, revealed the three anticipated failure mechanisms. For the transistors investigated these were distributed as follows.

BFW16A

Failures caused by storage were due to:
1) gold diffusion into the silicon,
2) degradation of the chip-to-package bond (only found after 100 hours at 350°C).

Failures caused by bottoming were caused by electro-migration from the emitter flap.

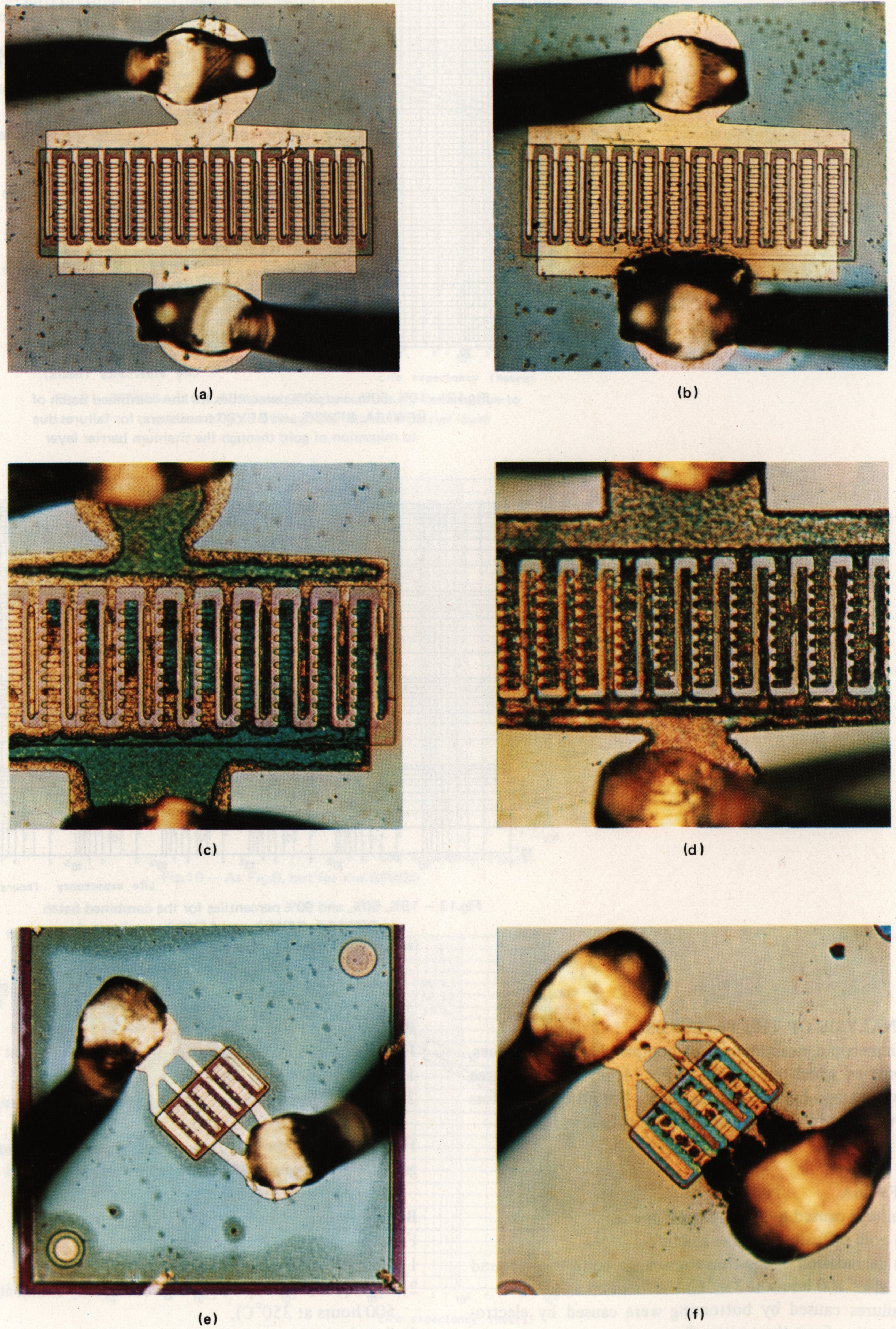
BFW30

Failures caused by storage were due to:
1) gold diffusion into silicon,
2) degradation of the chip-to-package bond (only found after 200 hours at 350°C).

Failures during the bottoming test occurred because of gold electro-migration in the emitter fingers.

BFY90

Failures caused by storage were due to:
1) gold diffusion into the silicon,
2) degradation of chip-to-package bond (only found after 500 hours at 350°C),
3) detached titanium-gold web.



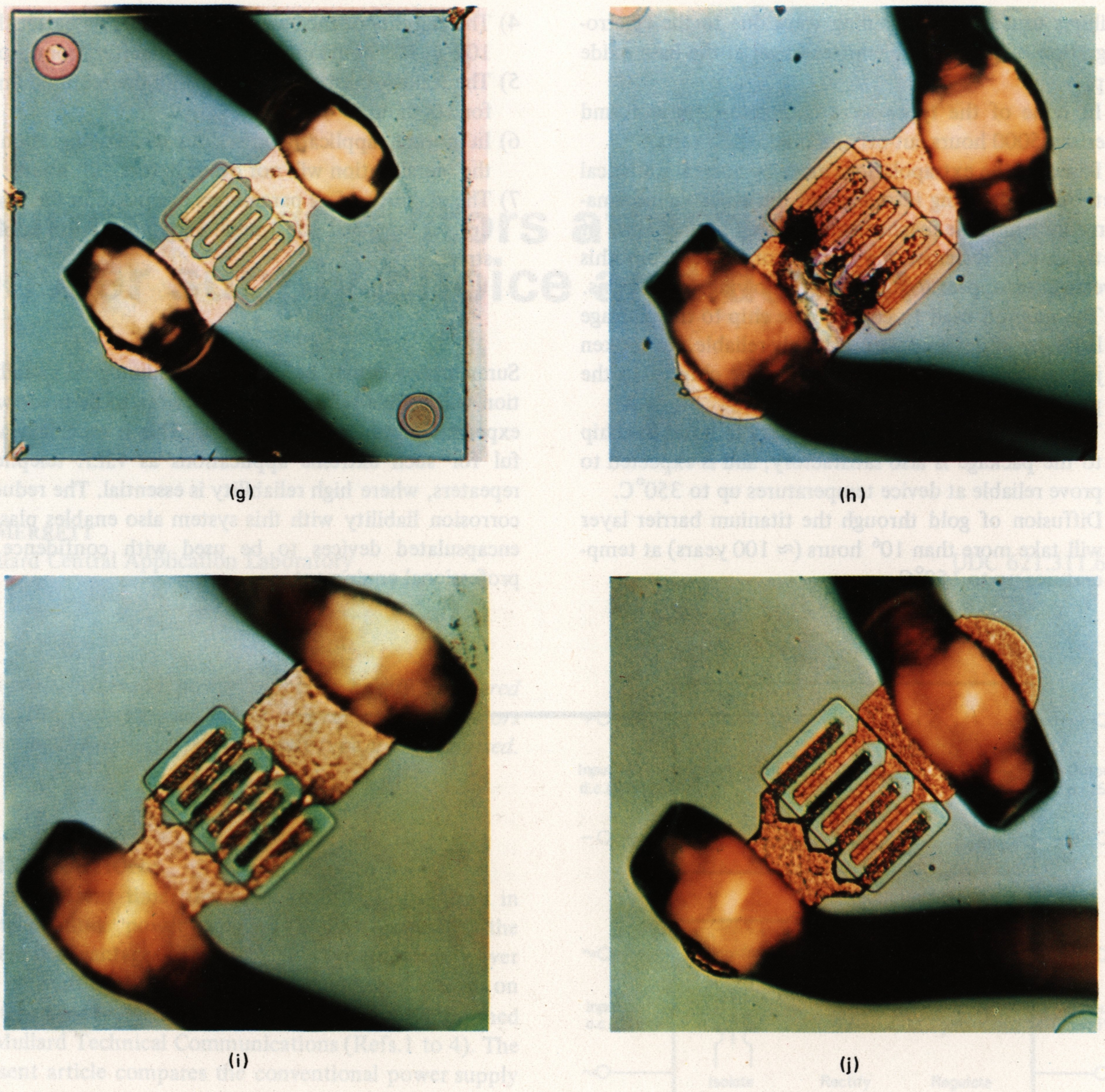


Fig.14 — Microphotographs of devices tested under accelerated life-test conditions:

(a) BFW16A before being tested. Chip dimensions 0.45mm × 0.45mm, 12 emitter fingers 6µm wide, 108 emitters, gold wedge-bonded connecting wires of 38µm

(b) BFW16A after passing a current of 1A for 2000 hours (electro-migration). Normal current rating 150mA

(c) BFW16A after storage at 275°C for 5000 hours. Normal storage temperature rating 200°C

(d) BFW16A after storage at 350°C for 100 hours. Normal storage temperature rating 200°C

(e) BFW30 before being tested. Chip dimensions 0.35mm × 0.35mm, 3 emitter fingers 6µm wide, 38 emitters, gold wedge-bonded connecting wires of 38µm

(f) BFW30 after passing a current of 300mA for 5000 hours (electro-migration). Normal current rating 50mA

(g) BFY90 before being tested. Chip dimensions 0.35mm × 0.35mm, 3 emitter fingers 4µm wide, gold wedge-bonded connecting wires of 38µm

(h) BFY90 after passing a current of 400mA for 5000 hours (electro-migration). Normal current rating 25mA

(i) BFY90 after storage at 275°C for 5000 hours. Normal storage temperature rating 200°C

(j) BFY90 after storage at 350°C for 200 hours. Normal storage temperature rating 200°C

Failures caused by bottoming were due to the electromigration of gold on the emitter finger at the base oxide step.

In none of the types were complete failures found after the 5000 hours cut-off and dissipation tests.

Based on the extrapolations made by normal statistical methods, and taking into account the available information concerning the mechanisms involved in the failure of metallisation systems, the results obtained from this investigation appear to justify the following conclusions.

1) The method used to connect the chip to the package leads, by 38μm gold wire, is highly reliable. No broken joints have been found, either to the chip or to the package leads.
2) The gold-silicon eutectic solder used to bond the chip to the package is also satisfactory, and is expected to prove reliable at device temperatures up to 350°C.
3) Diffusion of gold through the titanium barrier layer will take more than 10^6 hours ($\approx$ 100 years) at temperatures up to 150°C.
4) The stability of the base current should be better than 10% in 10^6 hours under normal operating conditions.
5) The leakage current remains within the required limits for 10^6 hours.
6) In normal applications, serious electro-migration of the metallisation will not occur before 10^6 hours.
7) The stability of all parameters examined in the tested devices remained good under all conditions of applied stress.

Summarising, it may be said that titanium-gold metallisation will enable semiconductor devices to be made with expected lifetimes of 10^6 hours. This is especially useful for such extreme applications as v.h.f. telephone repeaters, where high reliability is essential. The reduced corrosion liability with this system also enables plastic-encapsulated devices to be used with confidence in professional equipment.

Summary of factors affecting power supply choice and design

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UDC 621.311.68

The switched-mode power supply is briefly compared with the conventional power source, and the factors affecting the choice of power supply type are summarised.

INTRODUCTION

At the present time, there is a great deal of interest in switched-mode power supplies (SMPS) because of the inherent advantages offered by this type of supply over the conventional power source. A number of articles on switched-mode techniques have already been published in Mullard Technical Communications (Refs.1 to 4). The present article compares the conventional power supply with the switched-mode type, briefly discusses the advantages and disadvantages of both, and summarises the factors which affect the choice of power supply type.

A power supply can be defined as an item of equipment that accepts power from batteries or from the mains, and converts or modifies it for use in a particular part of the equipment. The input can be either d.c. from batteries or a.c. at 50Hz or some other frequency. The range of input voltages may be wide. The output is usually d.c. smoothed to give acceptably low ripple, and often has some form of regulation.

CONVENTIONAL POWER SUPPLIES

These fall into two groups: those for d.c. inputs and those for a.c. inputs. Both types are shown diagrammatically in Fig.1. Both are shown with regulators for the d.c. output as it is this class of power supply which can be readily compared with the switched-mode equivalent. The very simple power supply without regulator is unlikely, except in very special circumstances, to be considered for replacement by a switched-mode circuit as the cost will normally be too high and the facilities provided will be unnecessarily sophisticated.

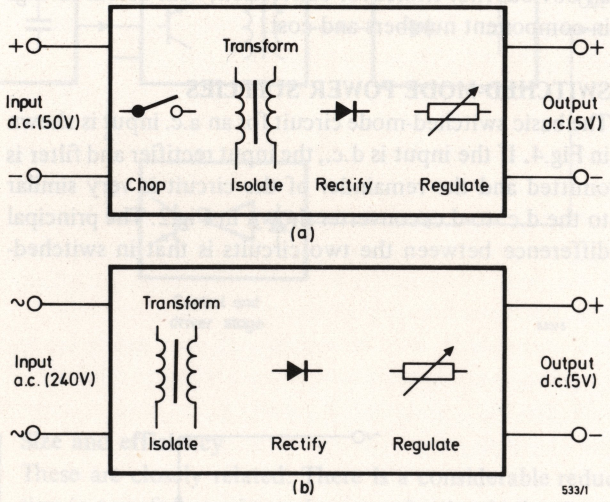

Fig.1a — Schematic diagram of d.c.-to-d.c. converter

Fig.1b — Schematic diagram of conventional a.c.-to-d.c. power supply

The conventional d.c.-to-d.c. converter is shown in more detail in Fig.2. This indicates the major components so that a comparison can be made with the switched-mode counterpart. In this circuit the input chopper merely interrupts the supply at a fixed (usually 1:1) mark-space ratio to enable the transformer to operate

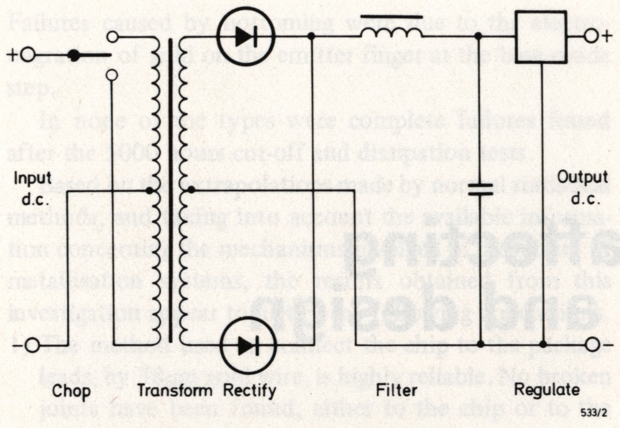

Fig.2 — Basic d.c.-to-d.c. converter circuit

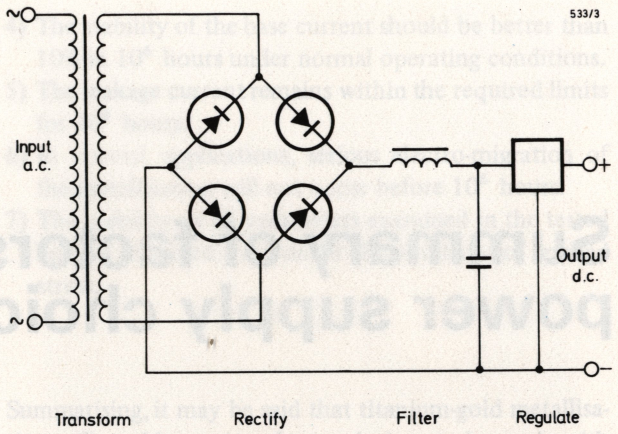

Fig.3 — Basic conventional a.c.-to-d.c. power supply circuit

from the d.c. input; what follows is much like the conventional a.c.-to-d.c. power supply, shown in Fig.3. It should be noted that the d.c.-to-d.c. converter is part way towards a full switched-mode system and is therefore an obvious first choice for conversion, with useful savings in component numbers and cost.

SWITCHED-MODE POWER SUPPLIES

The basic switched-mode circuit for an a.c. input is shown in Fig.4. If the input is d.c., the input rectifier and filter is omitted and the remainder of the circuit is very similar to the d.c.-to-d.c. converter shown in Fig.2. The principal difference between the two circuits is that in switched-mode operation the input chopper duty cycle is controlled in such a way that the output voltage is maintained at a constant value in spite of changes in supply voltage or load current. This is represented in Fig.4 by a feedback path from the output to the chopper. In this way the regulator can be dispensed with and by suitable design a number of other advantages also result.

With the introduction of high-voltage fast-switching transistors suitable for use as chopping elements, the switched-mode technique has become generally applicable to both battery and mains equipment. The rectified and smoothed 240V mains can now be used directly, so eliminating the need for a bulky 50Hz transformer.

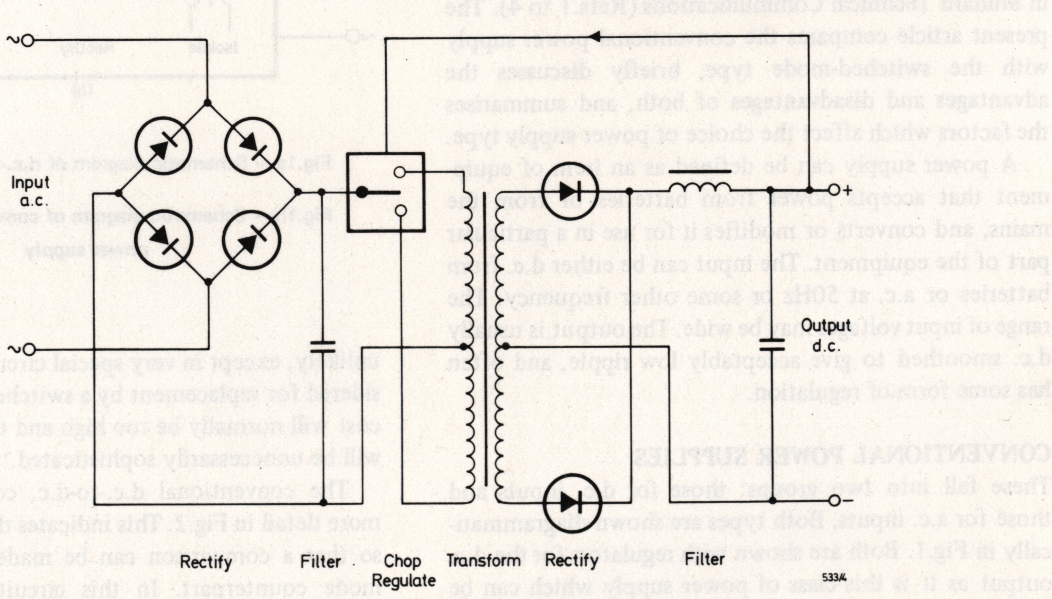

Fig.4 — Basic a.c.-input switched-mode power supply

Furthermore, the switching frequency can be raised to a minimum of 25kHz, so removing the nuisance effects of acoustic noise and at the same time allowing a reduction in the size of the transformer and easing the smoothing at the output, especially at low voltage and high current.

These factors lead either to cost reduction or other advantages which make the switched-mode power supply an interesting and often competitive alternative to more conventional power supplies.

ADVANTAGES AND DISADVANTAGES OF SMPS

The system block diagram of a switched-mode power supply is shown in Fig.5. The advantages and disadvantages of this type of supply compared with the conventional supplies shown in Figs.2 and 3 can be considered with respect to input, output, size, and efficiency.

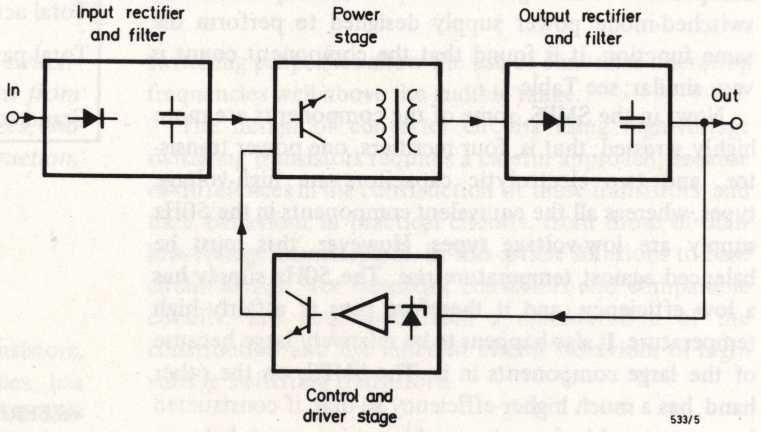

Fig.5 — A.C.-input switched-mode power supply system block diagram

Input

With a d.c. input, there is no basic difference between an SMPS and the d.c.-to-d.c. converter shown in Fig.2 as a chopper is required in both circuits. However, fast transistors enable the chopping frequency to be raised to 25kHz or higher, giving the added advantages of:

1) Smaller transformer.
2) No audible noise.

With an a.c. mains input, the advantages of an SMPS are:

1) Considerably smaller transformer.
2) 100Hz smoothing at 300V instead of at the low output voltage. This allows savings in capacitor size and cost (energy stored is proportional to CV^2, while the can volume is proportional to CV).
3) Operation over a large input voltage range, at least 1:2, and at 50 or 60Hz.

A disadvantage is that r.f.i. is generated but this can be kept within the limits defined in BS 800.

Output

The advantages of SMPS are:

1) Smoothing is much easier with a 25kHz ripple, especially at low voltage and high current. This allows considerable savings in cost, volume, and weight.
2) Regulator is more efficient.

Disadvantages are:

1) Basic smoothing of 100Hz and 25kHz ripple is easy but a special spike filter may be required to eliminate all traces of switching edges.
2) Regulation by feedback from the d.c. output includes the output filter components and their associated phase shifts. This limits the bandwidth of the feedback amplifier so that the transient response may not be as good as that of a conventional series regulator. However, the transient response is usually acceptable for most applications.

Size and efficiency

These are closely related. There is a considerable reduction in transformer size and some reduction in the size of the smoothing components. The other components are relatively small and the increased efficiency will reduce the heatsink requirements for the power transistors. The effect of this is that the volume of medium-power supplies can be reduced. A typical volume reduction would be:

6 cu in/W to 1 cu in/W (98·4ml/W to 16·4ml/W).

Linear dimension reduction ratio = 1·82:1,

and

area reduction ratio = 3·3:1.

Therefore, as cooling is proportional to surface area, to maintain the same temperature rise in the power supply box, the power loss in the box must be reduced by 3·3:1. This means that if a conventional 50Hz supply with series regulator has an efficiency of 50%, then the equivalent switched-mode supply must have an efficiency of 82%.

It therefore follows that if full use is to be made of the possibility of reduced size, the efficiency must be high. Fortunately the switched-mode method of control has a high efficiency, typically 75%, so by careful attention to layout and cooling, and optimisation of transformer winding and core design, it is possible to realise most of this potential.

RELIABILITY

Before discussing reliability in quantitative terms it is most important to be quite clear about definitions, and even then it is dangerous to make generalised statements as so much depends upon the actual equipment, its environment, and mode of operation. It is, however, possible to make some valid comments on a comparison between similar equipment constructed by alternative means.

If a quite standard 50Hz power supply with two independent series-regulated outputs is compared with a switched-mode power supply designed to perform the same function, it is found that the component count is very similar; see Table 1.

Now, in the SMPS, some of the components are more highly stressed; that is, four rectifiers, one power transistor, and two electrolytic capacitors are high-voltage types, whereas all the equivalent components in the 50Hz supply are low-voltage types. However, this must be balanced against temperature rise. The 50Hz supply has a low efficiency, and it therefore runs at a fairly high temperature. It also happens to be relatively large because of the large components in it. The SMPS, on the other hand, has a much higher efficiency so that, if constructed in a comparable box, it would run at a much lower temperature and hence have a relatively higher reliability.

In practice, advantage is taken of the smaller component size to reduce the overall dimensions, which leads to an increase in temperature. However, this should not be allowed to confuse the basic issue of comparison based on the system approach. It appears, therefore, that if all components are of equivalent quality and are run satisfactorily within their ratings at an equivalent temperature rise, there is no reason to suppose that there will be any significant difference in reliability between the two types.

TABLE 1

Comparison of Component Counts

Component Type	Component Numbers 50Hz PS	Component Numbers SMPS
Diodes, rectifiers	15	14
Transistors (small)	6	1
Transistors (power)	2	1
ICs	0	1
Capacitors (electrolytic)	7	4
Capacitors (others)	0	4
Resistors	14	8
Transformers	1	3
Input filter components	0	6
Total active	23	17
Total passive	22	25
Grand total	45	41

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Base circuit design for high-voltage switching transistors in power converters

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UDC 621.314.12: 621.3.032.271 [621.3.027.4]

Principles of base circuit design for high-voltage switching transistors in converter circuits are developed from investigation of the circuit behaviour of the devices, and supported by examination of their physical construction.

INTRODUCTION

The availability of fast high-voltage switching transistors, such as the BDY93, BDY96, and BU126 families, has created a rapidly-growing interest in the design of converters for power supply circuits. Because the breakdown voltage of these transistors is high (above 750 or 800V), they are suitable for operation direct from the rectified 220V or 240V mains supply. Furthermore, their fast switching properties allow the use of converter operating frequencies well above the audible range.

The design of converter circuits using high-voltage switching transistors requires a careful approach, because of differences in the construction of these transistors, and their behaviour in practical circuits, from those of their low-voltage counterparts. In this article solutions to base circuit design, for transistor converters and comparable circuits, are developed from a consideration of the construction and the inherent circuit behaviour of high-voltage switching transistors.

SWITCHING BEHAVIOUR

Fig.1 shows a complete period of typical collector voltage and current waveforms for a converter output transistor. The turn-on and turn-off intervals are indicated. The

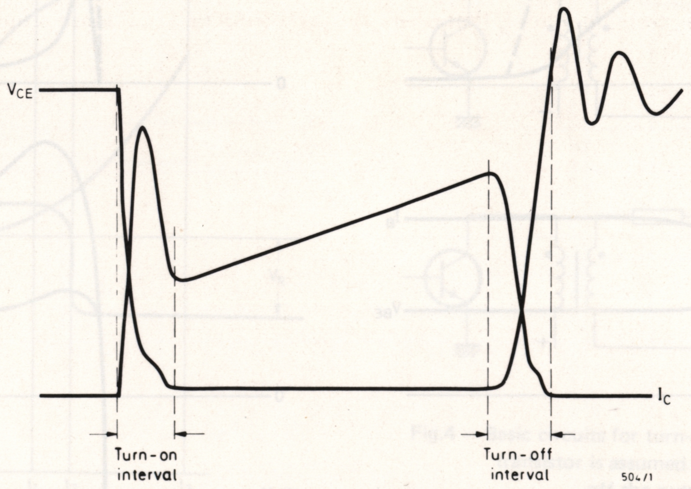


Fig.1 — Collector-emitter voltage and collector current waveforms during the conduction period of a converter output transistor

transient behaviour of the transistor during these two intervals, and the way it is influenced by the transistor base drive, will now be examined.

Turn-on behaviour

A particular set of voltage and current waveforms at the collector and base of a converter transistor during the turn-on interval is shown in Fig.2a. Such waveforms are found in a converter circuit in which a (parasitic) capacitance is discharged by a collector current pulse at transistor turn-on. The current pulse due to the discharge can be considered to be superimposed on the trapezoidal current waveform of basic converter operation.

A positive base current pulse I_B turns on the transistor. The collector-emitter voltage V_{CE} starts to decrease rapidly and the collector current I_C starts to increase. After some time, the rate of decrease of V_{CE} reduces considerably, and V_{CE} remains relatively high because of the large collector current due to the discharge of the capacitance. Thus the turn-on transient dissipation (shown by a broken line) reaches a high value.

The collector current later decreases to a trough before assuming the normal trapezoidal waveform, and there is again a rapid decrease in V_{CE}, which reaches the saturation value defined by the collector current and base current of the particular transistor.

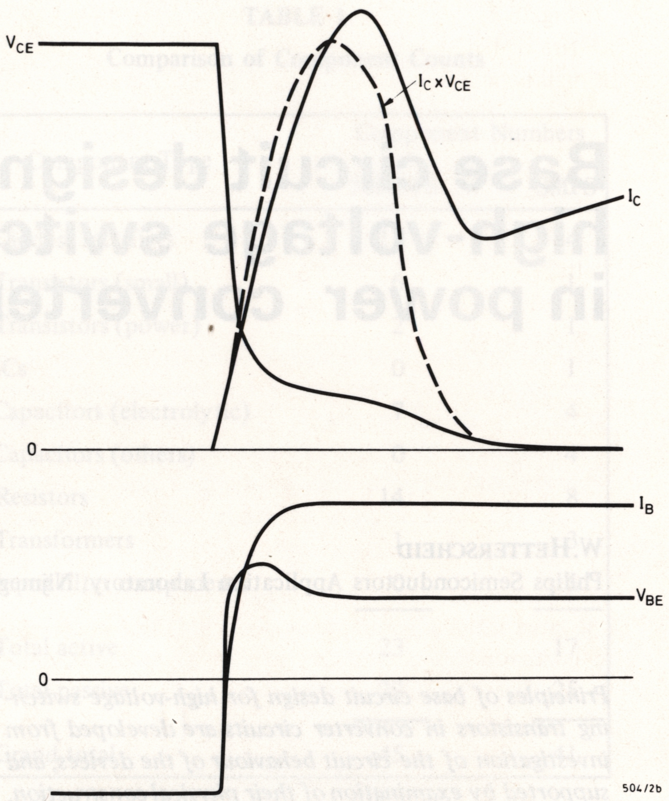


Fig.2b — Turn-on waveforms: fast-rising base current pulse

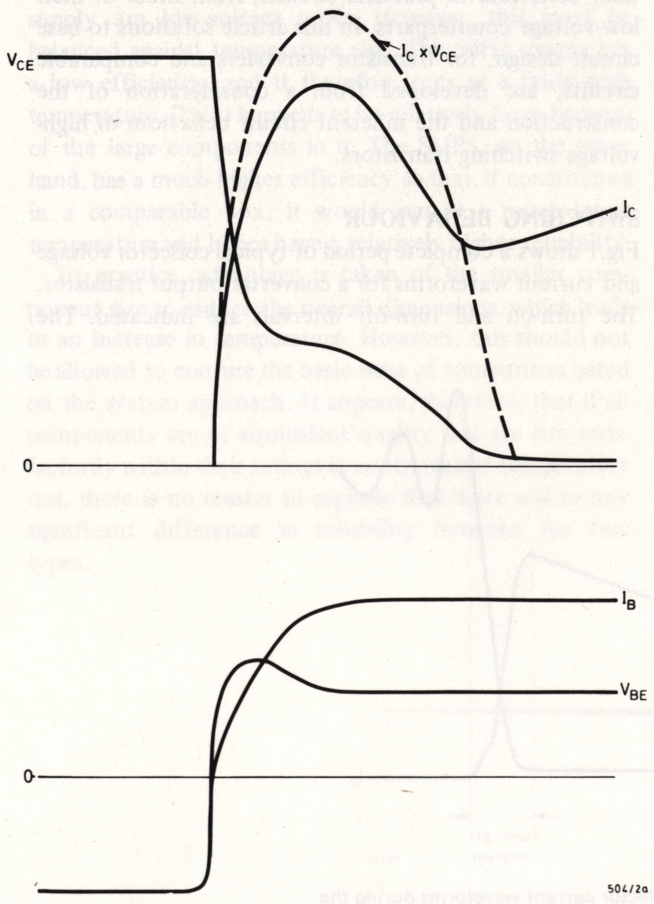


Fig.2a — Turn-on waveforms of a practical converter circuit

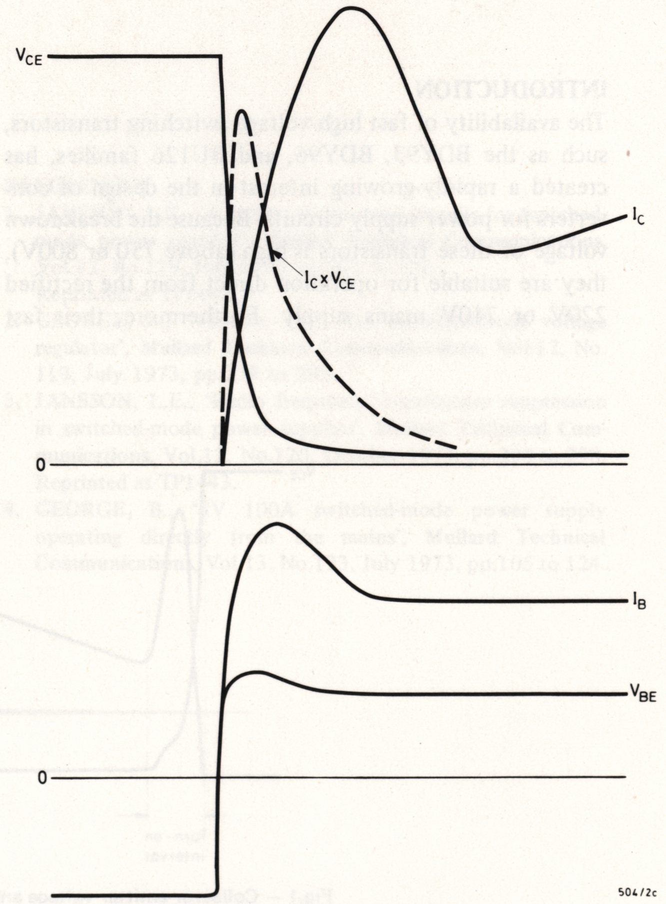


Fig.2c — Turn-on waveforms: very fast-rising base current pulse, with overshoot

Fig.2b depicts a similar situation but for a greater rate of rise of base current. The initial rapid decrease in V_{CE} is maintained until a lower value is reached, and it can be seen that the peak and average values of turn-on dissipation are smaller than they are in Fig.2a.

Fig.2c shows the effect on the transistor turn-on behaviour of a very fast-rising base current pulse which initially overshoots the final value. The collector-emitter voltage decreases rapidly to very nearly the transistor saturation voltage. The turn-on dissipation pulse is now lower and much narrower than those of Figs.2a and 2b.

From the situations depicted in Figs.2a, 2b, and 2c, it follows that for the output transistor of a converter circuit the turn-on conditions are most favourable when the driving base current pulse has a fast leading edge and overshoots the final value of I_B.

Turn-off behaviour

The waveforms which occur during the turn-off interval indicated in Fig.1 are shown on an expanded time-scale and with four different base drive arrangements in Figs.3a to 3d. These waveforms can be provided by base drive circuits as shown in Figs.4a to 4c: the circuit of Fig.4a provides the waveforms of Fig.3a; the circuit of Fig.4b those of Fig.3b and, with an increased reverse drive voltage, Fig.3c; the circuit of Fig.4c provides the waveforms of Fig.3d. The waveforms shown are typical of those found in the output stages of converters, and television horizontal deflection circuits, using high-voltage transistors.

In practical circuits, the waveform of the collector-emitter voltage is mainly determined by the arrangement of the collector circuit. The damping effect of the transistor on the base circuit is negligible except during the initial part of the turn-off period, when it only causes some delay in the rise of the V_{CE} pulse.

The $I_C \times V_{CE}$ (turn-off dissipation) pulse is dependent on both the transistor turn-off time and the collector current wave-shape during turn-off. Turn-off dissipation pulses are indicated in Figs.3a to 3d by dashed lines.

The circuit of Fig.4a incorporates a speed-up capacitor, an arrangement often used with low-voltage transistors. The effect of this is, as shown in Fig.3a, a very rapid decrease in the base current I_B, which passes through a negative peak value, and becomes zero at t_3. The collector current I_C remains virtually constant until the end of the storage time, at t_1, and then decreases reaching zero at t_3. The waveform of the emitter current I_E is determined by I_C and I_B, until it reaches zero at t_2, when the polarity of the base-emitter voltage V_{BE} is reversed.

After time t_2, when V_{BE} is negative and I_E is zero, the collector and base currents are equal and opposite, and

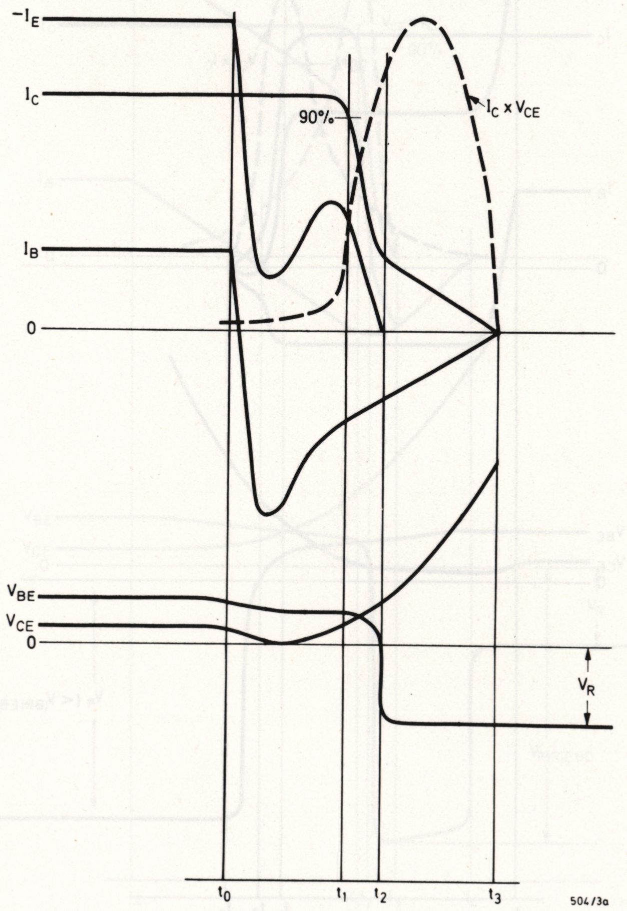


Fig.3a — Turn-off waveforms: circuit with speed-up capacitor

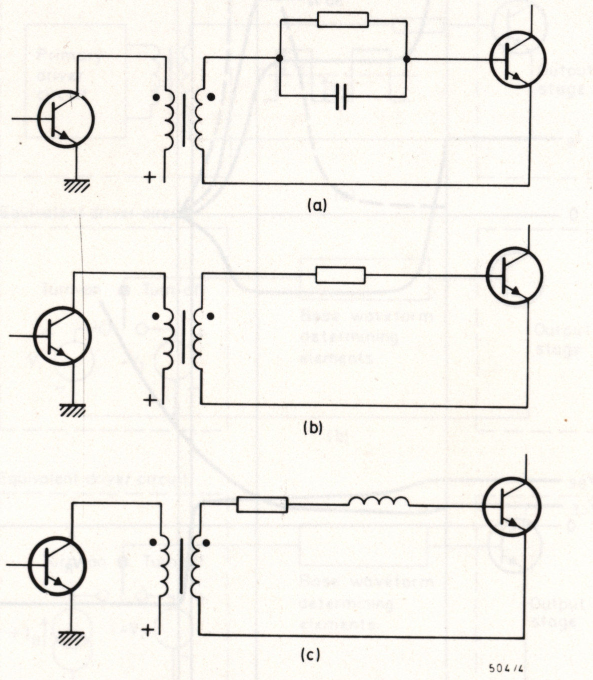


Fig.4 — Basic circuits for turn-off base drive. The driver transistor is assumed to be bottomed to turn off the output transistor.
(a) With speed-up capacitor
(b) Without speed-up capacitor
(c) With series inductor

the emitter is no longer effective. Thus the further decrease of collector current is governed by the reverse recovery process of the transistor collector-base diode. The reverse recovery 'tail' of I_C (from t_2 to t_3) is relatively long, and it is clear that the turn-off dissipation is high.

In the circuit of Fig.4b the capacitor is omitted. Fig. 3b shows that the negative base current is limited to a considerably lower value than in the previous case. All the currents I_B, I_C, and I_E reach zero at time t_3. The transistor emitter-base junction becomes reverse biased at t_2, so that during the short interval from t_2 to t_3 a small negative emitter current flows.

The emitter current, determined by the collector current and by the (driven) base current, therefore maintains control over the collector until it reaches zero. Furthermore, the collector current has a less pronounced tail and so the fall time is considerably shorter than that of Fig.3a. The turn-off dissipation is also lower than in the previous case.

Increasing the reverse base drive voltage in the circuit of Fig.4b, with the base series resistance adjusted so that the same maximum reverse base current flows, gives rise to the waveforms shown in Fig.3c. The collector current tail is even less pronounced, and the fall time shorter than in Fig.3b.

A further improvement in turn-off behaviour can be seen in the waveforms of Fig.3d, which are obtained by including an inductor in the base circuit as in Fig.4c. The rate of change of the negative base current is smaller than in the preceding cases, and the negative peak value of the base current is smaller than in Fig.3a. The collector current I_C reaches zero at t_3, and from t_3 to t_4 the emitter and base currents are equal. At time t_2 the polarity of V_{BE} is reversed and the base-emitter junction breaks down. At time t_4 the negative base-emitter voltage decreases from the breakdown value $V_{(BR)EBO}$ to the voltage V_R produced by the drive circuit.

The collector current fall time in Fig.3d is shorter than in any of the previous cases. The emitter current maintains control of the collector current throughout its decay. The large negative value of V_{BE} during the final part of the collector current decay drives the base-emitter junction into breakdown, and the junction breakdown voltage determines the largest possible reverse voltage. The turn-off of the transistor is considerably accelerated by the application, correctly timed, of this large negative base-emitter voltage, and the circuit gives the lowest turn-off dissipation of those considered.

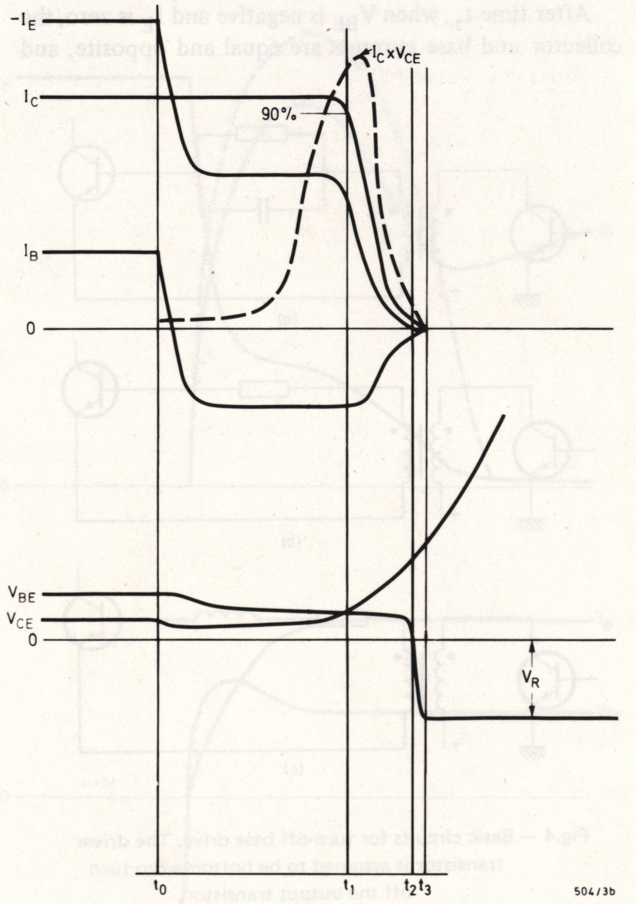


Fig.3b – Turn-off waveforms: circuit without speed-up capacitor

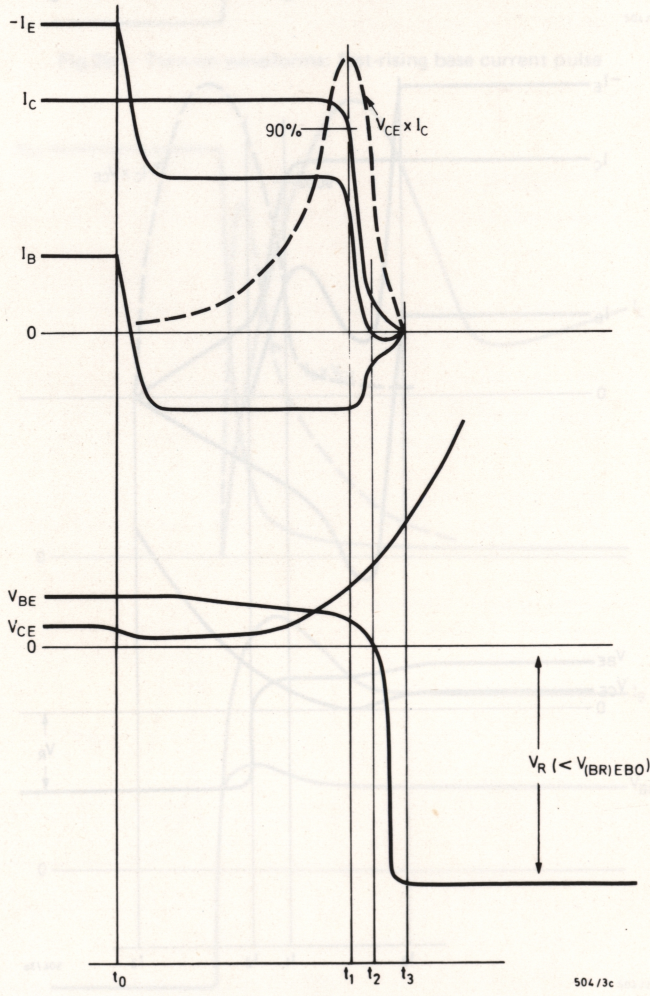


Fig.3c – Turn-off waveforms: circuit without speed-up capacitor, with increased reverse drive voltage

The operation of the base-emitter junction in breakdown during transistor turn-off, as shown in Fig.3d, has no detrimental effects on the behaviour of transistors in the BDY93, BDY96, BU205, BU208 and BU126 series. Published data on these transistors allow operation in breakdown as a method of achieving reliable turn-off, provided that the $-I_{B(AV)}$ and $-I_{BM}$ ratings are not exceeded.

It is evident from Figs.3a to 3d that the respective turn-off dissipation values are related by:

$$P_{off(a)} > P_{off(b)} > P_{off(c)} > P_{off(d)};$$

the fall times (related in each case to the interval from t_1 to t_3) by:

$$t_{f(a)} > t_{f(b)} > t_{f(c)} > t_{f(d)};$$

and the storage times (equal to the interval from t_0 to t_1) by:

$$t_{s(a)} < t_{s(b)} < t_{s(d)},$$

where the subscripts (a), (b), (c), and (d) refer to the waveforms of Figs.3a, 3b, 3c, and 3d, respectively. It follows that the circuit of Fig.4c, which provides the waveforms of Fig.3d, gives the most favourable turn-off power dissipation. It has, however, the longest storage time.

From consideration of the waveforms in Figs.3a to 3d, it can be concluded that optimum turn-off of a high-voltage transistor requires a sufficiently long storage time determined by the turn-off base current, and a sufficiently large negative base-emitter voltage correctly timed with respect to the collector current waveform.

The phenomena which have been described in this section become more pronounced when the temperature of the operating junction of the transistor is increased: in particular, the fall times and storage times are increased. The design of a base drive circuit should therefore be checked by observing the waveforms obtained at elevated temperatures.

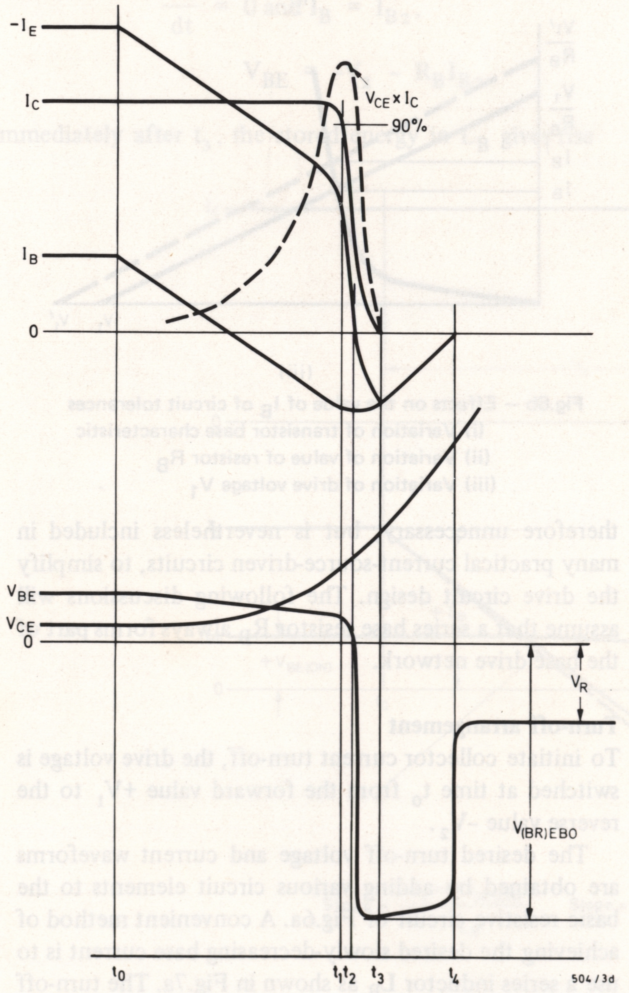
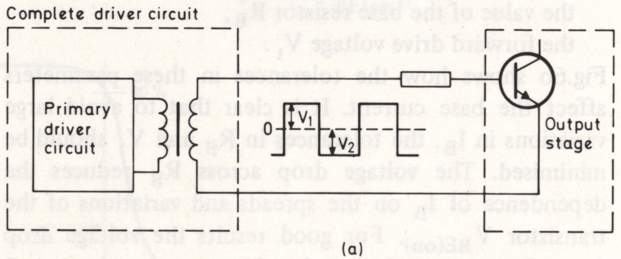
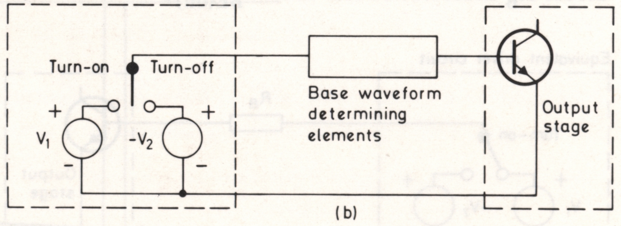


Fig.3d – Turn-off waveforms: circuit with series inductor

OPTIMUM BASE DRIVE CIRCUITRY

From the foregoing study of the required base current and base-emitter voltage waveforms, a fundamental base circuit arrangement to give optimum turn-on and turn-off of a high-voltage switching transistor will now be determined. It will be assumed that the driver stage is transformer-coupled to the base, as in Fig.5a, and that the driver transformer primary circuit is such that a low





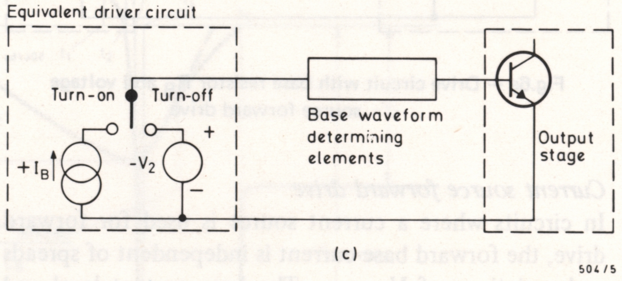


Fig.5a – Schematic drive circuit arrangement

Fig.5b – Equivalent drive circuit arrangement

Fig.5c – Equivalent circuit for current source forward drive

impedance is seen, looking into the secondary, during both the forward and reverse drive pulses. The complete driver circuit can then be represented as an equivalent voltage source of $+V_1$ volts during the forward drive period and $-V_2$ volts during the reverse drive/bias period. This is shown in Fig.5b.

Forward base drive can also be obtained from a circuit which acts as a current source rather than a voltage source. This situation, where the reverse drive is still obtained from a voltage source, is represented in Fig.5c. The basic circuit arrangements of Figs.5b and 5c differ only with respect to forward drive, and will where necessary be considered separately.

Comparable base drive waveforms can, of course, be obtained from circuits differing from those shown in Figs.5b and 5c. For such alternative circuit configurations the following discussion is equally valid.

Base series resistor

Most drive circuits incorporate a resistor R_B in series with the base. The influence of the value of this resistor on the drive characteristic will be briefly discussed.

Voltage source forward drive

In circuits with a voltage source for forward drive, shown in a simplified form in Fig.6a, the following parameters determine the base current:

the transistor base characteristic;
the value of the base resistor R_B;
the forward drive voltage V_1.

Fig.6b shows how the tolerances in these parameters affect the base current. It is clear that to avoid large variations in I_B, the tolerances in R_B and V_1 should be minimised. The voltage drop across R_B reduces the dependence of I_B on the spreads and variations of the transistor $V_{BE(on)}$. For good results the voltage drop across R_B must not be less than $V_{BE(on)}$.

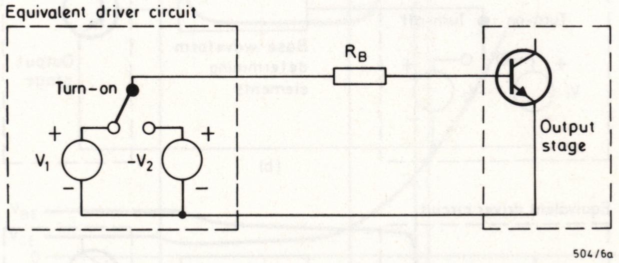


Fig.6a – Drive circuit with base resistor R_B and voltage source forward drive

Current source forward drive

In circuits where a current source is used for forward drive, the forward base current is independent of spreads and variations of $V_{BE(on)}$. The base current level and tolerances are governed entirely by the level and tolerances of the drive. A separate base series resistor is therefore unnecessary, but is nevertheless included in many practical current-source-driven circuits, to simplify the drive circuit design. The following discussions will assume that a series base resistor R_B always forms part of the base drive network.

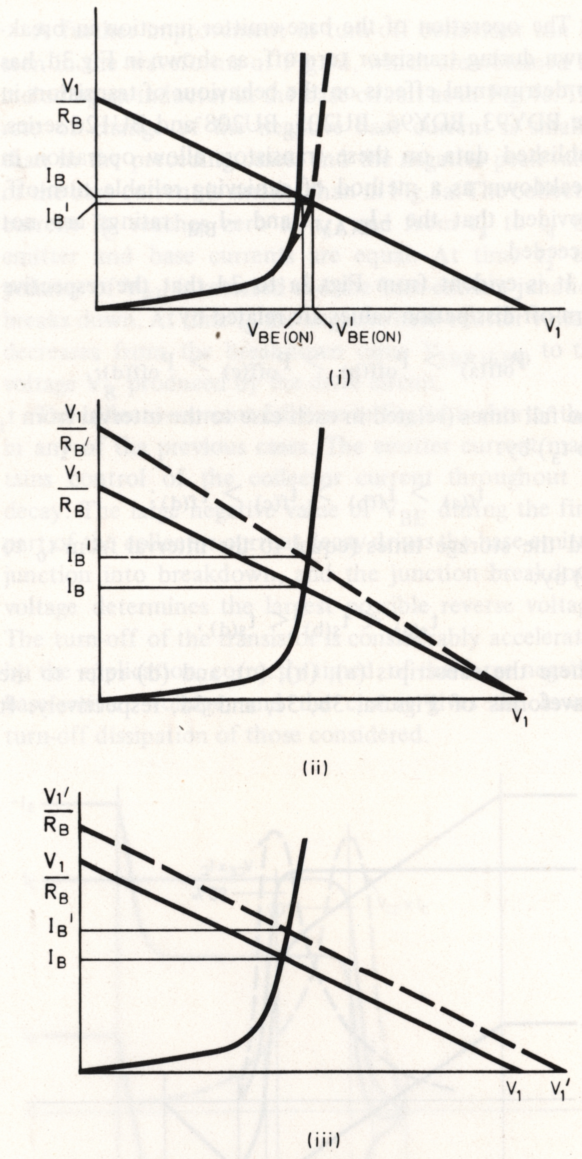


Fig.6b – Effects on the value of I_B of circuit tolerances
(i) Variation of transistor base characteristic
(ii) Variation of value of resistor R_B
(iii) Variation of drive voltage V_1

Turn-off arrangement

To initiate collector current turn-off, the drive voltage is switched at time t_0 from the forward value $+V_1$ to the reverse value $-V_2$.

The desired turn-off voltage and current waveforms are obtained by adding various circuit elements to the basic resistive circuit of Fig.6a. A convenient method of achieving the desired slowly-decreasing base current is to use a series inductor L_B as shown in Fig.7a. The turn-off waveforms obtained by this method are shown in Fig.7b.

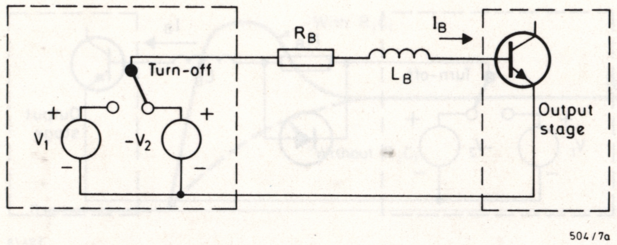


Fig.7a – Base drive circuit with series inductor

Base series inductor

At time t_0 the base current starts to decrease from the forward drive value I_{B1} with a slope equal to:

$$\frac{-V_2 - (+V_{BE(on)})}{L_B}.$$

For a considerable time after t_0, the (decreasing) input capacitance of the transistor maintains a charge such that there is no perceptible change in V_{BE}. At time t_2 the amount of charge removed by the negative base current $(-I_B)$ is insufficient to maintain this current, and its slope decreases.

At time t_3, when:

$$\frac{dI_B}{dt} = 0 \text{ and } I_B = I_{B2},$$

$$V_{BE} = -V_2 - R_B I_{B2}.$$

Immediately after t_3, the stored energy in L_B gives rise to a voltage peak tending to increase the reverse bias of the transistor. The voltage is clamped by the base-emitter breakdown voltage, so that:

$$V_{BE} = -V_{(BR)EBO}.$$

At time t_4 the negative base current starts to decrease with an initial slope equal to:

$$\frac{-V_2 + V_{(BR)EBO}}{L_B},$$

a positive quantity, and at t_5 it reaches zero. The base-emitter voltage then changes from $-V_{(BR)EBO}$ to the value $-V_2$, the level of the drive voltage.

As has been demonstrated, the collector storage time t_s is an important parameter of the drive circuit turn-off behaviour. Fig.7b shows that the value of t_s can be calculated approximately from:

$$\frac{-V_2 - (+V_{BE(on)})}{L_B} \cdot t_s = I_{B1} - I_{B2},$$

and this expression is sufficiently accurate in practice. In most cases the base current values are related by:

$$(-I_{B2}/I_{B1}) \approx 1 \text{ to } 3.$$

In the case where $(-I_{B2}/I_{B1}) = 2$, the collector storage time is given by:

$$t_s = \frac{3I_{B1}\, L_B}{-V_2 - (+V_{BE(on)})}.$$

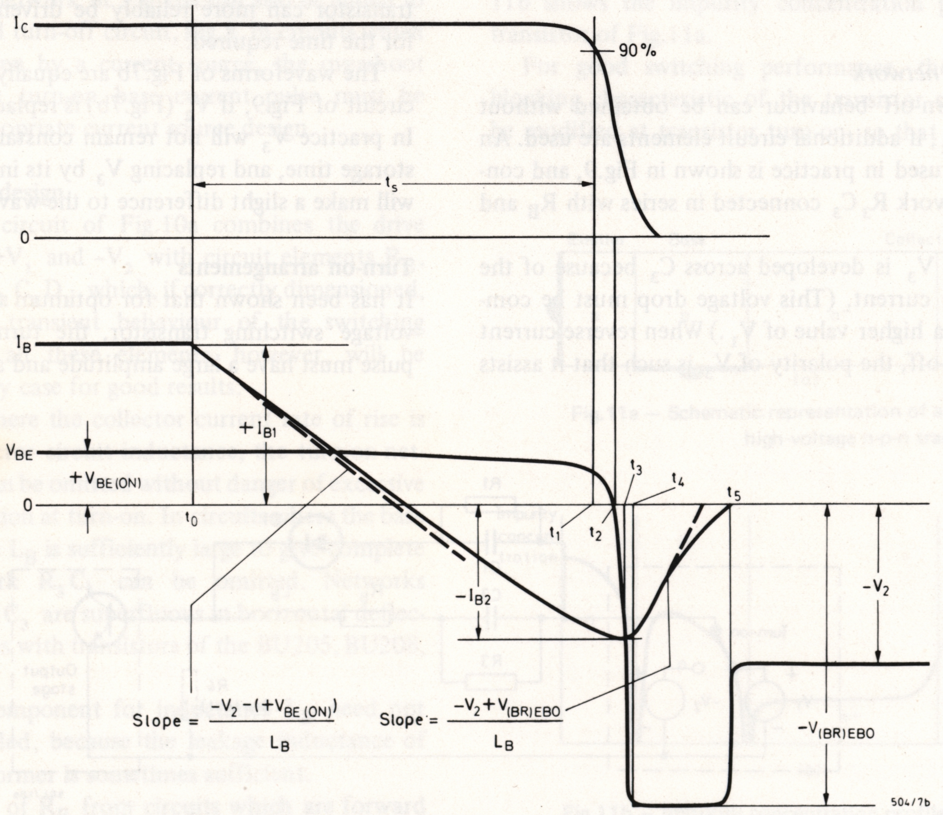


Fig.7b – Turn-off waveforms of the circuit of Fig.7a

In practical circuits, design considerations frequently indicate a relatively small value for V_2. The required value of t_s is then obtained with a small value of L_B, and consequently the energy stored in the inductor ($\frac{1}{2} L_B I_{B2}{}^2$) is insufficient to maintain the base-emitter junction in the breakdown condition. Fig.7b shows that breakdown should continue at least until the collector current is completely turned off. The higher the transistor junction temperature, the more stored energy is necessary to maintain breakdown throughout the increased turn-off time.

These phenomena are more serious in applications where the storage time must be short, as is the case for BDY93 and BDY96 transistors. For horizontal deflection output transistors such as the BU205 and BU208, which require a much longer storage time, the base inductance usually stores sufficient energy for correct turn-off behaviour.

Diode-assisted base inductor

It is possible to ensure the storage of sufficient turn-off energy by choosing a relatively large value for V_2. Where a driver transformer is employed, there is then a corresponding increase in V_1. To obtain the desired value of forward base current, the base resistance R_B must also be large. A large value of R_B, however, diminishes the effect of L_B on the transistor turn-off behaviour, unless R_B is bypassed by a diode as in Fig.8.

Turn-off RC network

Improved turn-off behaviour can be obtained without increasing V_2, if additional circuit elements are used. An arrangement used in practice is shown in Fig.9, and consists of a network R_3C_3 connected in series with R_B and L_B.

A voltage V_3 is developed across C_3 because of the forward base current. (This voltage drop must be compensated by a higher value of V_1.) When reverse current flows at turn-off, the polarity of V_3 is such that it assists the turn-off drive voltage V_2. Using the same approximation as before, the storage time is now given by:

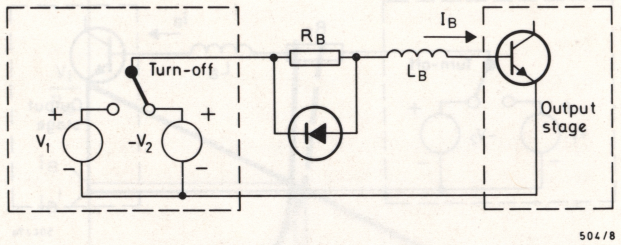


Fig.8 – Base drive circuit with diode-assisted series inductor

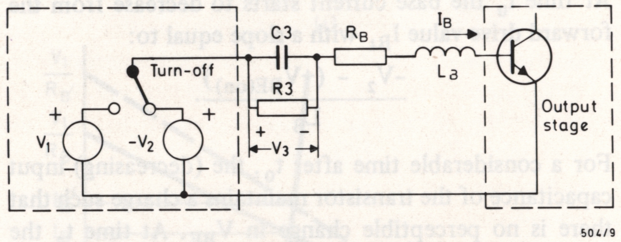


Fig.9 – Base drive circuit extended for improved turn-off behaviour

$$t_s = \frac{3I_{B1}\,L_B}{-(V_2 + V_3) - (+V_{BE(on)})} \,.$$

The same value of t_s now requires a larger value of L_B. The energy stored in L_B is therefore greater and the transistor can more reliably be driven into breakdown for the time required.

The waveforms of Fig.7b are equally applicable to the circuit of Fig.9, if V_2 (Fig.7b) is replaced by $(V_2 + V_3)$. In practice V_3 will not remain constant throughout the storage time, and replacing V_3 by its instantaneous value will make a slight difference to the waveforms.

Turn-on arrangements

It has been shown that for optimum turn-on of a high-voltage switching transistor, the turn-on base current pulse must have a large amplitude and a fast leading edge with overshoot. The inductance L_B included in the circuits derived for optimum turn-off (Figs.7 to 9), however, makes it difficult to produce such a turn-on pulse. The additional components (R_1, C_1, D_1) in the circuit of Fig.10a help to solve this problem, as shown by the waveforms of Fig.10b.

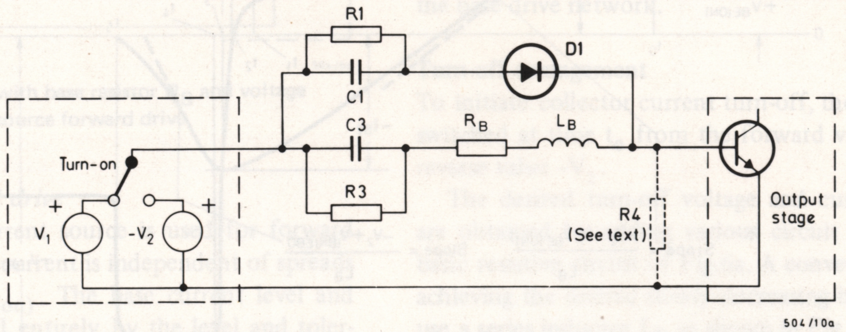


Fig.10a – Base drive circuit extended for improved turn-on behaviour with voltage source drive

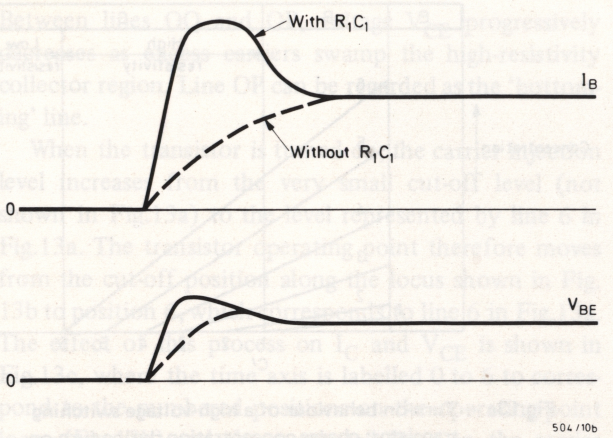


Fig.10b – Turn-on waveforms of the circuit of Fig.10a

At the instant of turn-on, network R_1C_1 in series with D_1 provides a steep forward base current pulse. The turn-off network is effectively bypassed during the turn-on period by C_1 and D_1. The time-constant R_1C_1 of the turn-on network should be chosen so that the forward current pulse amplitude is reduced virtually to zero by the time the transistor is turned on.

The turn-on network of Fig.10a can also be added to the diode-assisted turn-off circuit, Fig.8. In circuits which are forward driven by a current source, the overshoot required on the turn-on base current pulse must be achieved by appropriate current source design.

Practical circuit design

The base drive circuit of Fig.10a combines the drive voltage sources $+V_1$ and $-V_2$ with circuit elements R_B, L_B, R_3C_3, and $R_1C_1D_1$, which, if correctly dimensioned, allow optimum transient behaviour of the switching transistor. Not all these elements, however, will be necessary in every case for good results.

In circuits where the collector current rate of rise is limited by collector circuit inductance, the turn-on network $R_1C_1D_1$ can be omitted without danger of excessive collector dissipation at turn-on. In circuits where the base series inductance L_B is sufficiently large to give complete turn-off, network R_3C_3 can be omitted. Networks $R_1C_1D_1$ and R_3C_3 are superfluous in horizontal deflection output stages with transistors of the BU205, BU208, or similar series.

A discrete component for inductance L_B need not always be included, because the leakage inductance of the driver transformer is sometimes sufficient.

The omission of R_B from circuits which are forward driven by a voltage source should generally be considered bad design practice. It is, however, possible to select component values such that the functions of R_1C_1 and R_3C_3 are combined in a single network.

In some cases, the circuits of Figs.7a, 8, 9, and 10a may generate parasitic oscillations (ringing). These can usually be eliminated by connecting a damping resistor R_4 between the transistor base and emitter, as shown in broken lines in Fig.10a.

PHYSICAL BEHAVIOUR OF HIGH–VOLTAGE SWITCHING TRANSISTORS

Base circuit design for high-voltage switching transistors will now be considered with respect to the physical construction of the devices. To achieve a high breakdown voltage, the collector includes a thick region of high-resistivity material. This is the major difference in the construction of high- and low-voltage transistors.

The construction of a triple-diffused high-voltage transistor is represented schematically in Fig.11a. The collector region of an n-p-n transistor comprises a high-resistivity n^- region and a low-resistivity n^+ region. Most of the collector voltage is dropped across the n^- region. For semiconducting material of a chosen resistivity, the thickness of the n^- region is determined by the desired collector breakdown voltage. The thickness of the n^+ region is determined by technological considerations, in particular the mechanical construction of the device. Fig. 11b shows the impurity concentration profile of the transistor of Fig.11a.

For good switching performance, the high-voltage blocking characteristic of the transistor structure must be modified at transistor turn-on, so that a low forward

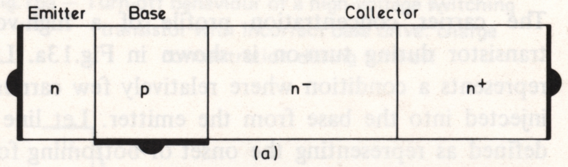


Fig.11a – Schematic representation of a triple-diffused high-voltage n-p-n transistor

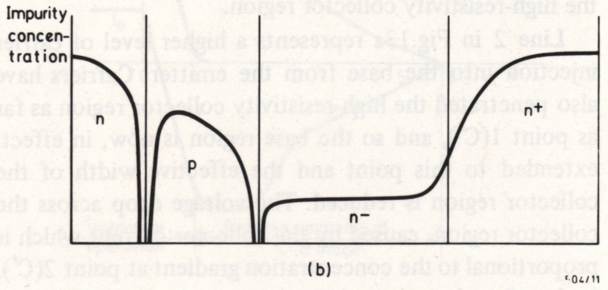


Fig.11b – Impurity concentration profile of the transistor of Fig.11a

voltage condition is exhibited. One method of achieving this is to inject a large number of carriers through the base into the collector region. The high resistivity of the n⁻ region is then 'swamped' by excess carriers. This effect is often referred to as collector-width modulation.

The following discussion of the physical changes which occur at transistor turn-on and turn-off is based on a much simplified transistor model; that is, the one-dimensional charge-control model. Fig.12 shows such a model of a low-voltage transistor, and assumes a large free carrier-to-doping concentration ratio in the base due to the carriers injected from the emitter. Line a represents the free carrier concentration in the base for transistor operation in the active region ($V_{CB} > 0$), and line c that for the bottomed condition ($V_{CB} < 0$). Line b represents the concentration at the onset of bottoming, where $V_{CB} = 0$. The slope of the free carrier concentration line at the collector junction is proportional to the collector current density, and therefore to the collector current.

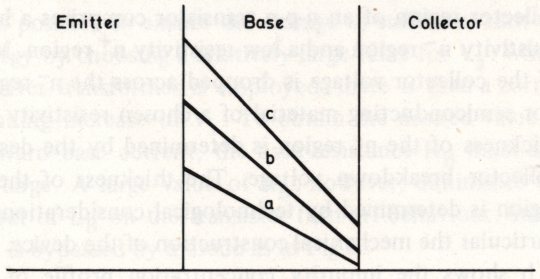


Fig.12 — Charge-control representation of a low-voltage transistor: in the active region (line a); at the onset of bottoming (line b); and in the heavily bottomed state (line c)

Turn-on behaviour

The carrier concentration profile of a high-voltage transistor during turn-on is shown in Fig.13a. Line 1 represents a condition where relatively few carriers are injected into the base from the emitter. Let line 1 be defined as representing the onset of bottoming for the metallurgic collector junction; that is, point 1(C′). In this case $V_{C'B} = 0$, whereas the externally measured collector voltage is very high, because of the voltage drop across the high-resistivity collector region.

Line 2 in Fig.13a represents a higher level of carrier injection into the base from the emitter. Carriers have also penetrated the high-resistivity collector region as far as point 1(C′), and so the base region is now, in effect, extended to this point and the effective width of the collector region is reduced. The voltage drop across the collector region, caused by the collector current which is proportional to the concentration gradient at point 2(C′), is therefore less than the voltage drop which occurred with the level of carrier injection on line 1.

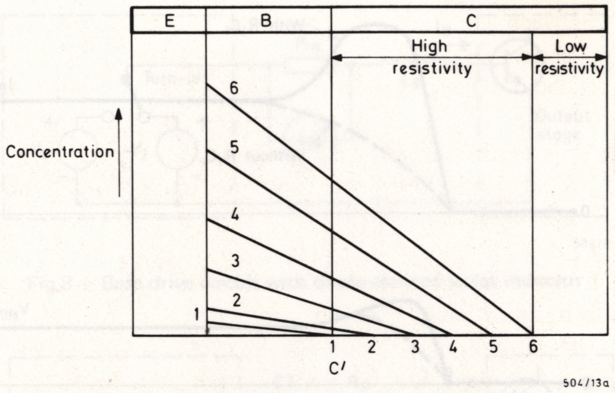


Fig.13a — Turn-on behaviour of a high-voltage switching transistor: charge concentration during turn-on

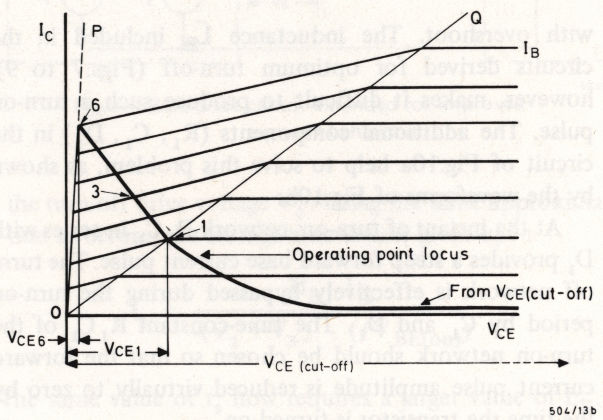


Fig.13b — Turn-on excursion locus

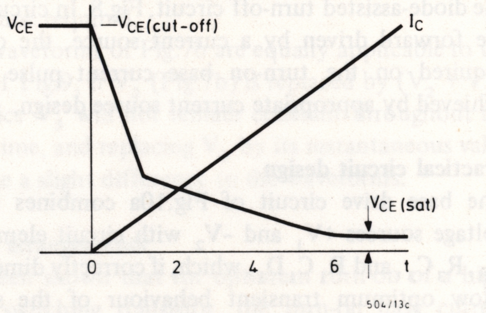


Fig.13c — Turn-on waveforms

Lines 3, 4 and 5 represent still higher carrier injection levels, and hence decreasing effective collector widths. The voltage drop across the effective collector also decreases.

In the situation represented by line 6, the entire high-resistivity collector region has been flooded with excess carriers. The collector-base voltage is therefore so low that the transistor is effectively bottomed. The low bottoming voltage has been obtained at the expense of a large base current, and this explains why a high-voltage transistor has a low current gain, especially at large collector currents.

Fig.13b shows simplified collector current/voltage characteristics for a typical high-voltage transistor.

Between lines OQ and OP, voltage V_{CE} progressively decreases as excess carriers swamp the high-resistivity collector region. Line OP can be regarded as the 'bottoming' line.

When the transistor is turned on, the carrier injection level increases from the very small cut-off level (not shown in Fig.13a) to the level represented by line 6 in Fig.13a. The transistor operating point therefore moves from the cut-off position along the locus shown in Fig. 13b to position 6, which corresponds to line 6 in Fig.13a. The effect of this process on I_C and V_{CE} is shown in Fig.13c, where the time axis is labelled 0 to 6 to correspond to the numbered positions on the operating point locus (Fig.13b) and the numbered lines on the carrier concentration diagram (Fig.13a).

The time taken to reach the emitter injection level 6 (Fig.13a) is directly proportional to the turn-on time of the transistor. The rate of build-up of emitter injection depends on the peak amplitude and rise-time of the turn-on base current pulse. The shortest turn-on time is obtained from a large-amplitude base current pulse with a fast leading edge. Thus, physical considerations support the conclusion already drawn from a study of the circuit behaviour of the transistor.

Turn-off behaviour

The carrier concentration in the saturated transistor at the beginning of the turn-off period is represented by line 0 in Fig.14a, corresponding to line 6 in Fig.13a. As shown in Fig.14b, the base current I_B gradually decreases, but I_C remains almost constant for some time, and $-I_E$ therefore decreases to match I_B. The resulting carrier concentration patterns are shown as lines 1 and 2 in Fig. 14a. This process is plotted against time in Fig.14b where, again, the graduation of the horizontal axis corresponds to that of the lines in Fig.14a.

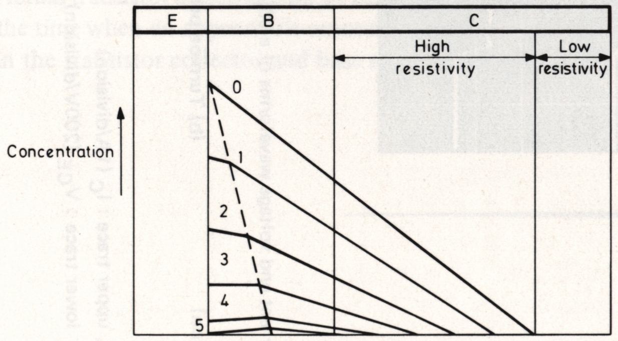


Fig.14a — Turn-off behaviour of a correctly-driven high-voltage switching transistor: charge concentration during turn-off

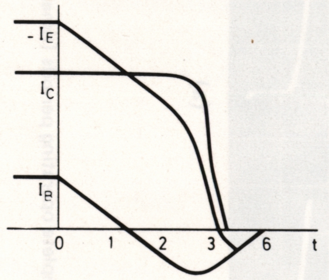


Fig.14b — Turn-off waveforms

At time point 3 the emitter current has reduced to zero, and is slightly negative until point 6. Thus the carrier concentration lines 4 and 5 have negative slope. Complete collector current cut-off is reached before point 6. (This situation is not represented in Fig.14a.)

Excess carriers present in the collector region are gradually removed from point 0 onwards. This results in increasing collector voltage, because of the increasing effective width of the high-resistivity collector region.

Figs.14a and 14b depict a typical turn-off process giving good results with high-voltage transistors: the waveforms of Fig.14b should be compared with those of Figs.3d and 7b. A different process is shown in Figs.15a and 15b. The initial situation is similar (line 0, Fig.15a) but the base current has a steep negative slope. At time

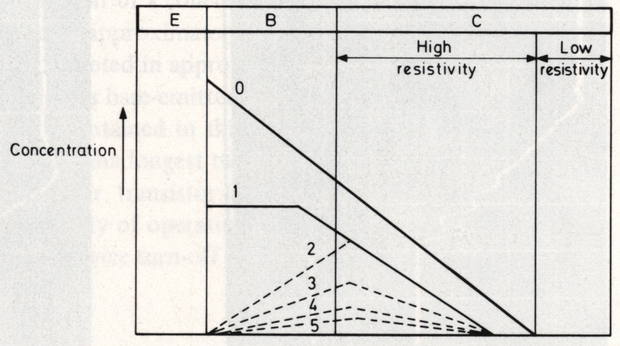


Fig.15a — Turn-off behaviour of a high-voltage switching transistor with incorrect base drive: charge concentration during turn-off

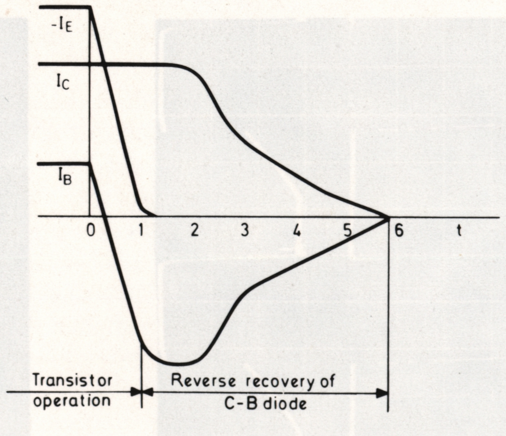


Fig.15b — Turn-off waveforms

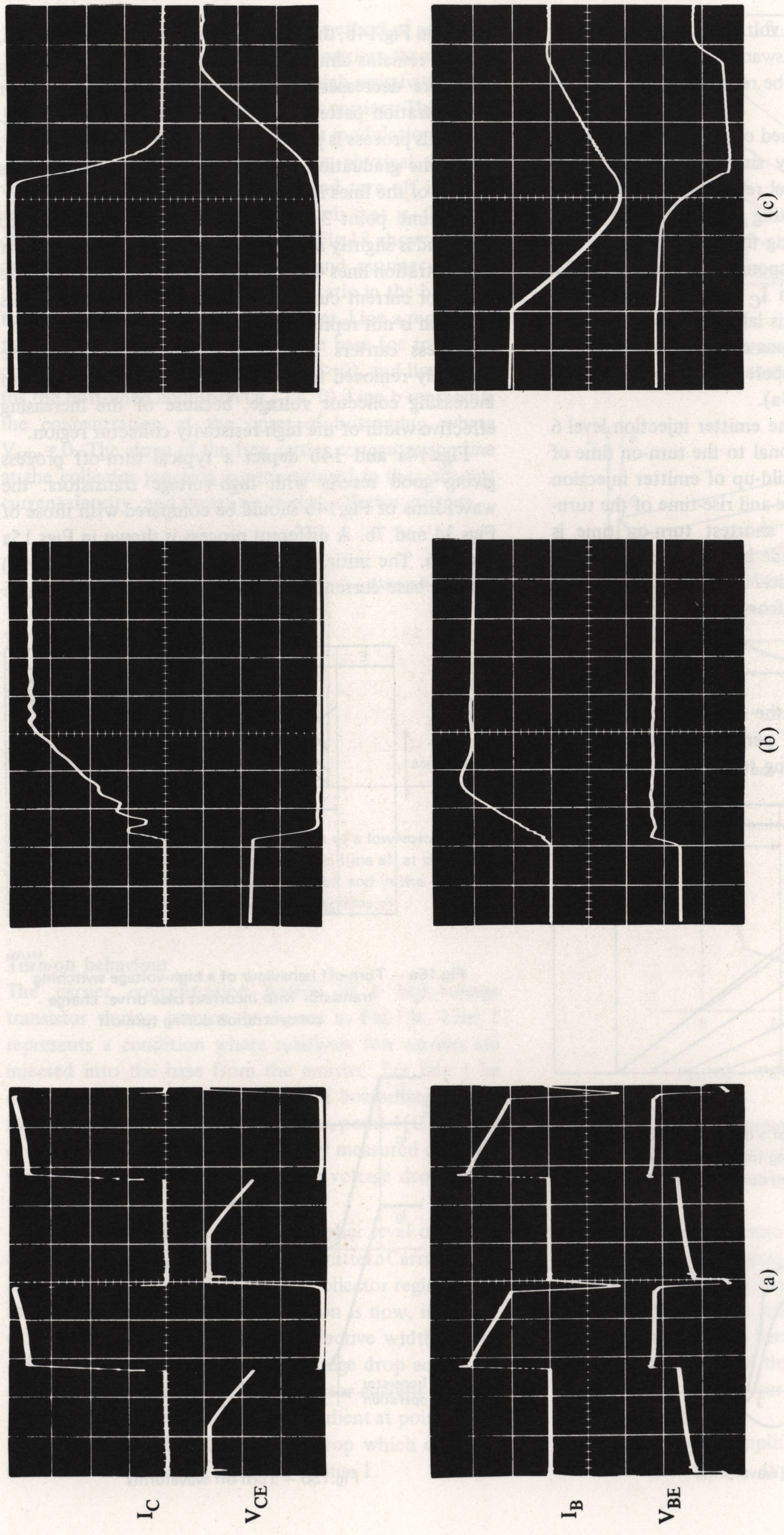


Fig.16 — Current and voltage waveforms of a 500W forward converter using an experimental switching transistor

(a) Two complete operating periods (timebase: 10μs/division) (b) Turn-on period (timebase: 0·5μs/division) (c) Turn-off period (timebase: 0·5μs/division)

Upper photographs, upper trace : I_C (1A/division) lower trace : V_{CE} (200V/division)

Lower photographs, upper trace : I_B (500mA/division) lower trace : V_{BE} (5V/division)

point 1 of Fig.15b, the emitter current $-I_E$ has reached zero, and so the carrier concentration line 1 has zero slope at the emitter junction. The emitter-base junction is effectively cut off and only the relatively small leakage current (not shown in Fig.15b) is flowing. From point 1 onwards, therefore, the emitter has no influence on the behaviour of the transistor. The switching process is no longer 'transistor action', but the reverse recovery process of a diode. The carrier concentration pattern during this process is shown in Fig.15a in broken lines, with zero slope at the emitter junction because the emitter is inoperative.

The reverse recovery process is slow, because of the high resistivity of the collector region and the consequent slow decrease of collector current. (Collector and base currents are, of course, equal and opposite when the emitter is cut off). The turn-off dissipation increases progressively as the transition time from collector saturation to cut-off increases. Furthermore, at higher junction temperatures the reverse recovery charge, and hence the duration of the recovery process, is greater.

The longer the turn-off time, then, the greater the turn-off dissipation, and hence the higher the device temperature which itself causes a further increase in turn-off time and dissipation. To avoid the risk of thermal runaway and subsequent transistor destruction which arises under these conditions, the turn-off drive must be such that no part of the turn-off is governed by the reverse recovery process of the collector-base diode. Actual transistor action should be maintained throughout the time when an appreciable amount of charge is present in the transistor collector and base regions, and therefore the emitter should continue to operate to remove the excess charge.

There are many conditions of transistor turn-off which lie between the extreme cases of Figs.14a and 15a. Circuits in which the operating conditions tend towards those shown in Fig.15a must be regarded as a potential source of unreliability, and so the performance of such circuits at elevated temperatures should be carefully assessed.

PRACTICAL CONVERTER OSCILLOGRAMS

The voltage and current waveforms of Fig.16 are those of a single-transistor forward converter with an output power of 500W, using an experimental high-voltage transistor. Fig.16a shows two complete operating periods, and Figs.16b and 16c show, respectively, the turn-on and turn-off periods on expanded time-scales. This converter circuit embodies the turn-on and turn-off drive design philosophy developed in this article.

Turn-on losses are minimised by the shape of the turn-on base current pulse, which has a leading edge considerably faster than that of the collector current.

The arrangement of the turn-off base drive is such that the storage time is sufficiently long to prevent the formation of a collector current 'tail'. In fact the storage time is approximately 1·7μs. Collector current turn-off is completed in approximately 0·5μs. During turn-off the transistor base-emitter junction is driven into breakdown, and maintained in this condition for 1·5μs, sufficient to capture the longest turn-off time that can occur with the particular transistor used. In calculating this time, the possibility of operation at high temperatures, and spreads in the device turn-off time, have been taken into account.

Cores for switched-mode power supply transformers

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UDC 621.3.042.1 [621.311.6]

The design of a range of cores for transformers to operate at ultrasonic frequencies in switched-mode power supplies is described. Design information for transformers capable of supplying load powers of up to 500W is given.

INTRODUCTION

The need for a range of cores for high-frequency power transformers has arisen because of the increasing popularity among power supply manufacturers of the switched-mode technique. This technique, utilising the present generation of high-voltage switching semiconductor devices, can provide a small, light, efficient power supply capable of self-regulation over a wide range of input voltages and load currents.

In a switched-mode power supply the bulky, silicon iron-cored mains-frequency transformer of the conventional power supply is replaced by a much smaller, ferrite-cored transformer operating at ultrasonic frequency. This frequency, typically 25kHz, is obtained by solid-state switching of the input voltage which may be d.c. or roughly-smoothed rectified a.c. The power supply output may be either d.c. or a.c. at any required voltage. Typical applications are logic supplies where rectified mains or 50V d.c. is converted to 5V d.c.; and public transport fluorescent lighting supplies where 28V d.c. is inverted to 240V a.c. (25kHz).

Transformers for these power supplies have until now utilised E-cores and pot cores from existing product ranges. Each of these solutions has its disadvantages. Pot cores are relatively expensive, and have been designed for low flux density, low current inductor applications: the slots are unsuitable for the terminations of high-current carrying conductors. The majority of existing E-cores, also expensive and difficult to assemble, have centre poles of rectangular section. These cause conductor bowing and excessive turn length, and therefore increased leakage inductance and copper loss.

A range of ferrite cores has been designed specifically for use in switched-mode power supplies, inverters, and converters. The core design has been optimised for operation in push-pull circuits at frequencies up to 50kHz. At present the range comprises four versions: types FX3720, FX3730, FX3740, and FX3750, covering the range of d.c. load powers from <50 to 500W. To ensure that a wide range of operating requirements can be met, each core is capable of 150% rated power throughput at an ambient temperature of 60°C. Under these conditions and with minimum cooling (radiation and free convection only), the maximum core temperature rise is 40degC.

BASIC CORE REQUIREMENTS

The basic requirements that the cores must fulfil dictate the material from which they are made, and their general shape.

Core material

The most suitable core material for this application is considered to be A16. This material has a high value of saturation flux density and low hysteresis loss, and both these properties are guaranteed up to an operating temperature of 100°C which is the maximum recommended for the cores without derating. In Fig.1 the maximum hysteresis loss (P_m) of A16 material is plotted against flux density, for a frequency of 25kHz.

Other important properties exhibited by this material are high resistivity, giving low eddy current core loss at high flux densities and frequencies, and high Curie temperature (200°C). Material A16 has lower hysteresis loss and higher resistivity than A9, the material previously recommended for power applications.

Core shape

Ideally, any transformer operating at high flux density and high frequency should be completely screened, to minimise external magnetic fields and radiation. This is especially true for miniaturised equipment, where volume-to-power output ratios of the order of 40×10^3 mm^3/W are attained. Pot cores, of course, satisfy this requirement, but the slots impose restrictions on the size of conductors which can be accommodated. The combination of U- and I-cores, on the other hand, offers ease of access for winding but has the disadvantage of a relatively larger external field.

The E-core geometry with a centre pole of circular section (Fig.2) has been selected as the basis of the new range. This core, virtually a pot-core with two sides removed, has some of the advantages of both pot- and U-cores, and its external magnetic leakage can have an acceptably low value. The circular centre pole minimises the winding turn length for a given cross-sectional area, thus reducing copper losses. Conductor bowing is eliminated, assisting the achievement of low leakage inductance, and giving a compact winding.

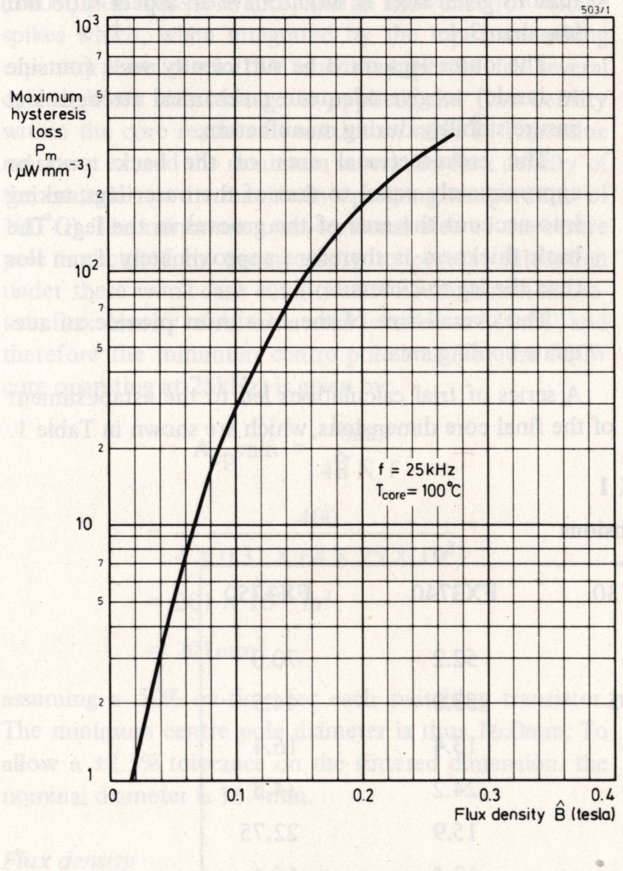

Fig.1 — Maximum hysteresis loss P_m of A16 material plotted against flux density B

For assembly, grooves have been provided in the outer poles to accept standard readily-available metric studding. This avoids the necessity for special clips or attachments. The grooves can be seen in Fig.2. An additional fixing hole through the centre pole was initially considered, but this would have led to an unacceptable increase in the winding turn length and therefore in copper loss.

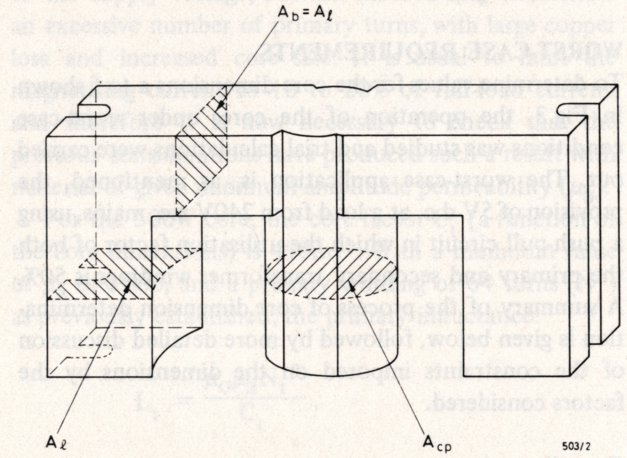

Fig.2 — FX3700 series core geometry

CORE DIMENSION OPTIMISATION

Because of the variety of constraints and specifications to be met by the cores, the final core sizes were obtained by optimisation of the dimensions to ensure efficient operation in the worst-case condition.

Worst-case condition

The worst-case application is considered to be operation in a switched-mode power supply with a push-pull circuit, supplying 5V d.c. to the load at the rated power output from 240V a.c. mains input. In such a circuit an additional 2.5V is required at the transformer secondary terminals, to allow for losses in rectifier diodes, smoothing and filtering circuits, and distribution cables, and therefore the transformer is required to pass 50% more power than the supply delivers to the load. Furthermore, half of both windings are non-conducting at any instant (assuming full-wave rather than full-wave-bridge rectification), and the secondaries comprise strip conductors, and so the winding area and power handling capabilities required for this application are considered adequate to satisfy the majority of other applications.

Certain dimensions of the cores were established by the requirements of the above worst-case application.

The effects upon such important parameters as core factor, overall volume, power throughput, etc., of minor dimensional changes were then examined using h.f. transformer theory. Experimental constants were incorporated, and the E-shape assumed.

Core temperature rise is an important design parameter, and a suitable value must be chosen. The temperature rise of the core in operation must be sufficiently high to permit a good power/volume ratio to be obtained, but not high enough to cause degradation of the transformer materials. A maximum core temperature of 100°C was chosen, and an ambient temperature of 60°C assumed. Thus, a maximum core temperature rise of 40degC was used in the optimisation.

WORST-CASE REQUIREMENTS

To determine values for the core dimensions a to f shown in Fig.3, the operation of the cores under worst-case conditions was studied and trial calculations were carried out. The worst-case application is, as mentioned, the provision of 5V d.c. at a load from 240V a.c. mains, using a push-pull circuit in which the utilisation factor of both the primary and secondary transformer windings is 50%. A summary of the process of core dimension determination is given below, followed by more detailed discussion of the constraints imposed on the dimensions by the factors considered.

Core dimensions

The secondary winding required for a low-voltage output (in this case 7.5V to allow for circuit losses) must be a small integral number of turns. Given this number, the centre pole diameter is fixed by flux density considerations. Tooling and pressing techniques led to the decision to make the 'stack height' dimension (labelled f in Fig.3) equal to the centre pole diameter. The remaining dimensions were chosen to satisfy the following practical considerations.

The window area must allow for the winding, the insulation, creepage distance, and the coil former. For reasons given later it should have an aspect ratio not less than 3:1.

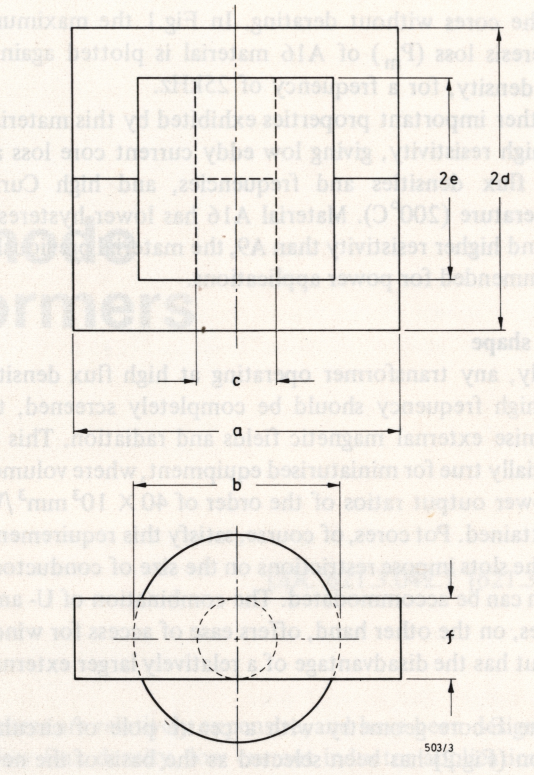

Fig.3 — Simplified core and coil former geometry

The outer legs must be sufficiently wide (outside to inside) to give adequate mechanical strength and ensure stability during manufacture.

The cross-sectional area of the back must be approximately equal to that of the outer legs, taking into account the area of the grooves in the legs. The back thickness is therefore approximately 1mm less than the leg thickness.

The overall size of the core must provide an adequate cooling area.

A series of trial calculations led to the establishment of the final core dimensions, which are shown in Table 1.

TABLE 1

Core Dimensions

Dimension	FX3720	FX3730	FX3740	FX3750
a	34.5	40.6	52.2	70.0
b	22.75	27.05	33.0	44.5
c	9.5	11.6	13.4	16.4
d	17.3	19.5	24.2	34.5
e	12.25	13.9	15.9	22.75
f	9.5	11.6	13.4	16.4

All dimensions are in millimetres

The foregoing outline of the evolution of a set of core dimensions will now be amplified, with particular reference to the FX3750 core which is designed for load powers up to 500W.

Secondary voltage

To provide 5.0V d.c. at the terminals of a distant load, 7.5V d.c. is required at the transformer secondary terminals. Because of the large secondary current, strip conductors with a small integral number of turns are essential, and experience with trial designs suggested that the transformer secondary should comprise 2 + 2 turns.

Primary voltage

The turns ratio is determined by the minimum mains input voltage. Allowing for various mains voltage standards, losses in mains filters and in rectifiers, and the saturation voltage of the switching transistor, the minimum d.c. voltage appearing across the transformer primary is considered to be 240V. The turns ratio throughout the range of cores is thus fixed at 240:7.5, that is 32:1, and for the 500W core this necessitates a primary winding of 64 + 64 turns.

The absolute maximum voltage appearing across the transformer primary is assumed to be 400V d.c. This value comprises the nominal U.K. mains peak voltage (340V) plus 10% tolerance, and an allowance for voltage spikes which, when integrated by the input smoothing capacitor, can reach 25V and may persist for several cycles. When this voltage is applied, the flux density within the core reaches its maximum value $\hat{B}$. This value must not exceed the minimum saturation flux density of the material (at its maximum operating temperature of 100°C). The minimum cross-sectional area of the centre pole is dictated by the necessity to prevent saturation under these worst-case conditions. The minimum saturation flux density of A16 material is taken as 310mT, and therefore the minimum centre pole area (for the 500W core operating at 25kHz) is given by:

$$A_{cp}\text{min} = \frac{E_{max}}{4\hat{B}\,N_1\,f},$$

$$= \frac{400}{4 \times 0.31 \times 64 \times 25 \times 10^3},$$

$$= 201 \times 10^{-6}\ \text{m}^2,$$

$$= 201\text{mm}^2,$$

assuming a 50% on-time for each switching transistor. The minimum centre pole diameter is thus 16.0mm. To allow a ±2.5% tolerance on the sintered dimension, the nominal diameter is 16.4mm.

Flux density

The need to prevent core saturation under transient voltage conditions dictates the minimum centre pole diameter, as shown above. Under normal operating conditions, the flux density is much lower and the design is core-loss limited. The centre pole area has been determined by the transient voltage condition, the number of primary turns, and the saturation flux density of the material, and so it is necessary at this stage of the design procedure to check the core losses, to ensure that the permitted temperature rise is not exceeded.

Magnetising current

In any transformer it is desirable to make the magnetising current as small as possible. A small magnetising current can be obtained by presenting a large primary inductance to the supply voltage, but this method may necessitate an excessive number of primary turns, with large copper loss and increased core size. It is usual to limit the magnetising current to 10 to 20% of full-load current, and therefore it is now necessary to check that the previous considerations have produced such a result with material of given minimum amplitude permeability (μ_a).

For the 500W core, the core factor C_1 (a function of the core dimensions) is 498m^{-1}. With a minimum value of μ_a of 1000, and a primary winding of 64 turns (N_1) as previously established, the primary inductance:

$$L_1 = \frac{\mu_o \mu_a N_1{}^2}{C_1},$$

$$= \frac{4\pi \times 10^{-7} \times 1000 \times 64^2}{498},$$

$$= 10.3 \times 10^{-3}\text{H},$$

$$= 10.3\text{mH}.$$

Operating at 25kHz and with a primary voltage of 240V, the mark/space ratio of the primary voltage waveform is 1:1, giving the peak-to-peak magnetising current:

$$I_{pk-pk} = \frac{Et_{on}}{L_1},$$

$$= \frac{240 \times 20 \times 10^{-6}}{10.3 \times 10^{-3}},$$

$$= 0.466\text{A},$$

$$= 466\text{mA}.$$

That is, the peak magnetising current is 233mA.

Since the maximum output power is 750W and assuming 90% efficiency, the maximum full load primary current:

$$I_1 = \frac{750}{240 \times 0.9},$$

$$= 3.5\text{A}.$$

Thus, the core factor, centre pole area, and number of primary turns can be seen to meet both the magnetising current and the transient flux density requirements.

Creepage and clearance specifications

Various national and international standards and recommendations, such as IEC65, IEC335, and BS415:1972, lay down, for stipulated voltages, minimum creepage and clearance distances between core, terminations, and windings, for all unimpregnated isolation transformers. The majority of these standards can be met by careful design of coil formers and terminations. At mains voltages, a creepage distance of 8.0mm is required between mains windings and any windings or screens that are accessible to a user. For this reason, the internal length e (Fig.3) of each core must exceed half the desired winding breadth by 4.0mm.

To obtain low leakage inductance, a broad and shallow window area is required. This also leads to low values of a.c. winding resistance. A window area aspect ratio of 3:1 is considered a desirable minimum value.

Cooling area

When the maximum core temperature rise is 40degC above ambient, the total surface area of the core and winding will dissipate the heat generated by core and copper losses at the specific rate of 520µWmm^{-2}, assuming a uniform temperature distribution throughout the core. The total surface area of the core and winding, therefore, must be sufficient to dissipate the total transformer loss at this rate.

Consideration of transformer losses and the cooling area required, as well as the mechanical strength of the core, determined that the back and the outer limbs should be of larger cross-sectional area than the centre pole.

TRANSFORMER ANALYSIS

An analysis was carried out to relate the core power throughput capability, and other important properties, to the simplified dimensions shown in Fig.3. Although parameter values obtained may not be accurate in the absolute sense, the values given for various sets of core dimensions will be correct relative to each other. The analysis thus provides a reliable means of estimating the relative effects of small changes of core dimensions, and can be confidently employed to optimise the dimensions given by the method described above. The analysis is based on h.f. transformer theory and could be of use in the design of other types of transformer core; it will therefore be given in detail below.

Basic relations

For a ferrite-cored power transformer operating at a high frequency, the design is determined by core loss considerations, rather than by the saturation flux density limitations that occur at low frequencies. It has been shown (Ref.1) that:

$$P_{tot}{}^2 = \frac{16\,P_{out}{}^2\, m\,\rho_c\,F_R}{(R_p)_1\;F_a} \times \frac{\ell_e \ell_w}{A_e A_a}, \qquad \text{... (1)}$$

where:

P_{tot} = total transformer loss,
P_{out} = transformer output power,
ρ_c = resistivity of copper at 20°C,
m = fractional rise in ρ_c at temperatures above 20°C,
F_R = fractional rise in winding resistance due to copper eddy currents,
$(R_p)_1$ = normalised parallel loss resistance due to core losses,
F_a = winding copper area/total window area,
ℓ_w = mean turn length,
A_e = effective magnetic path area,
ℓ_e = effective magnetic path length, and
A_a = total window area.

Grouping the parameters that must be assumed, let:

$$K_a = \frac{m\,\rho_c\,F_R}{(R_p)_1\;F_a}, \qquad \text{... (2)}$$

and so:

$$P_{tot} = 4\,P_{out}\sqrt{K_a} \times \sqrt{\frac{\ell_e \ell_w}{A_e A_a}}. \qquad \text{... (3)}$$

Let P_h be the specific rate of heat transfer in watts per unit area of cooling surface. This factor is dependent on the permitted temperature rise and the method of cooling. If A_c is the total surface area of core and winding available for cooling, then:

$$P_{tot} = P_h\,A_c, \qquad \text{... (4)}$$

and

$$\frac{P_h}{4\,P_{out}\sqrt{K_a}} = \sqrt{\frac{\ell_e \ell_w}{A_c{}^2\,A_e\,A_a}},$$

$$= \sqrt{\frac{C_1\,\ell_w}{A_c{}^2\,A_a}}, \qquad \text{... (5)}$$

where C_1 is a core factor given by:

$$C_1 = \frac{\ell_e}{A_e}.$$

In Eq.5, the left-hand side expresses requirements and assumptions, and the right-hand side expresses the core and winding geometry.

From Eq.5:

$$P_{out} = \frac{P_h\,A_c}{4\sqrt{K_a}} \cdot \sqrt{\frac{A_a}{C_1\,\ell_w}}. \qquad \text{... (6)}$$

A value for $P_h/4\sqrt{K_a}$ can now be obtained from assumptions, and a direct relationship between output power and geometry obtained.

From Ref.2, the specific dissipation (assuming only radiation and free convection, and a mean surface temperature 40degC above ambient) is $P_h = 0.52 \times 10^{-3}$ W mm^{-2}. Now:

m = 1.3 for a winding temperature of 100°C,
ρ_c = $1.7 \times 10^{-5}\ \Omega$ mm,
F_R = 1.8 (estimated),
F_a = 0.2 (estimated), and
$(R_p)_1$ = 2.5Ωmm^{-1} for material A16 at f = 25kHz and B = 200mT.

Therefore, from Eq.2:

$$K_a = \frac{1.3 \times 1.7 \times 10^{-5} \times 1.8}{2.5 \times 0.2} = 79.6 \times 10^{-6};$$

and from Eq.6:

$$P_{out} = \frac{0.52 \times 10^{-3}}{4 \times 8.92 \times 10^{-3}} \times A_c \cdot \sqrt{\frac{A_a}{C_1\,\ell_w}},$$

$$= 1.46 \times 10^{-2} \times A_c \cdot \sqrt{\frac{A_a}{C_1\,\ell_w}}. \qquad \text{... (7)}$$

Thus for any given set of core dimensions, the output power may be estimated. Although, because of the uncertainty of the assumptions, the answer may not be correct in absolute terms, it will give a reliable guide to the relative effects of core proportion changes.

Core geometry properties

Other properties of the core can be derived from the core geometry. The simplified geometry of Fig.3 is used, and the core is assumed fully wound.

Ferrite volume V_f

$$V_f = 2f\,(ad - be) + \frac{\pi c^2 e}{2}\ \text{mm}^3.$$

Copper volume V_c

$$V_c = \frac{\pi e\,F_a\,(b^2 - c^2)}{2}\ \text{mm}^3,$$

where: $F_a = 0.2$ (assumed).

Core factor C_1

$$C_1 = 2e\left[\frac{1}{f\,(a-b)} + \frac{4}{\pi c^2}\right] + \frac{(b-c)}{2f\,(d-e)} + \frac{\pi}{4f} + \frac{\pi\,(d - e + 0.5959c)}{4f\,(d-e) + \tfrac{1}{2}\pi c^2}\ \text{mm}^{-1}.$$

Mean turn length ℓ_w

$$\ell_w = \frac{\pi\,(b+c)}{2}\ \text{mm}.$$

Overall window area A_a

$$A_a = e\,(b-c)\ \text{mm}^2.$$

Total cooling area of core and winding A_c

$$A_c = 2f\,(a+2d) + 4\,(ad - be) + \pi\left(2be + \frac{b^2}{2}\right)\left\{\frac{1 - 2\arctan\,[f/\sqrt{(b^2 - f^2)}]}{\pi}\right\} - f\sqrt{(b^2 - f^2)} + 4e\,[b - \sqrt{(b^2 - f^2)}]\ \text{mm}^2.$$

Overall rectilinear volume of core and winding V_o

$$V_o = 2abd\ \text{mm}^3.$$

Output power P_{out}

$$P_{out} = 1.46 \times 10^{-2} \times A_c\sqrt{(A_a/C_1\,\ell_w)}\ \text{W}.$$

Power per unit volume

$$\text{Power per unit volume} = \frac{P_{out}}{V_o}\ \text{W mm}^{-3}.$$

Surface power dissipation

Surface power dissipation for 40degC temperature rise

$$= 0.520 \times 10^{-3} \times A_c\ \text{W}.$$

TRANSFORMER REALISATION AND EVALUATION

Using the technique described, core dimensions were obtained for transformers capable of meeting the worst-case requirements in 50W, 100W, 200W, and 500W power supplies. Sample cores having these dimensions were produced by slitting and grinding blocks of A16 material. The cores were then wound and assembled, and appraised under operating conditions in the appropriate circuits.

Temperature rise measurements, set out in Table 2,

TABLE 2
Results of Temperature Measurements

Core	Frequency (kHz)	T_{amb} (°C)	V_{in} (d.c.)	Winding temperature rise (degC)	Core temp. rise (degC) centre pole	top	outside leg	V_{out} V(d.c.)	I_2 (A)	P_{out} (W)	Winding
FX3730	25	24	300	36	40	24	21	5	20	100	Conventional push-pull
	25	25	300	19	25	–	–	5	20	100	Single-ended push-pull
	25	25	300	14	16	–	–	5	20	100	Single-ended push-pull with split primary winding: 1st half-primary; 2nd secondary; 3rd half-primary
	25	28	240	16	17	–	–	5	20	100	
	25	21	300	28	27	–	–	5	27	135	
	25	23	300	48	46	–	–	5	36	180	
	25	26	300	37	36	–	–	5	30	150	
FX3740	25	22	240	31	47	29	20	5	40	200	Conventional push-pull: lst primary; 2nd secondary
	25	29	300	29	46	27	17	5	40	200	
	25	31	300	–	47	28	22	5	40	200	As above, but with core ends covered to prevent convection cooling
	25	30	300	20	25	–	–	5	40	200	Single-ended push-pull with split primary winding: 1st half-primary; 2nd secondary; 3rd half-primary
	25	31	240	22	27	–	–	5	40	200	
	25	24	240	26	35	–	–	5	40	200	Conventional push-pull, split as above
	25	25	300	25	34	–	–	5	40	200	
	35	32	240	18	21	–	–	5	40	200	Single-ended push-pull, split as above
	35	25	300	16	21	–	–	5	40	200	
	35	26	350	16	22	–	–	5	40	200	
	25	25	240	33	47	–	–	5	40	200	Single-ended push-pull: 1st primary; 2nd secondary
	25	28	300	32	46	–	–	5	40	200	
FX3750	25	25	240	9	14	13	7	5	37	185	Conventional push-pull: 1st half-primary; 2nd secondary; 3rd half-primary
	25	22	245	42	39	35	22	5.1	98	500	

Note: the values of temperature rise given in Table 2 were obtained using sample cores, and are to be taken as typical. Results obtained with production cores may vary.

show that the cores meet the worst-case design requirement of a maximum temperature rise of 40degC.

The test conditions were changed, for the purpose of this investigation, by increasing the input voltage, increasing the switching frequency from 25 to 35kHz, and raising the ambient temperature. Changing the test conditions produced very small variations in the temperature rise, well within the limits of experimental error.

The effect of an increase in frequency is to reduce both the core flux density and the penetration depth of the winding copper. The combined effect of increased frequency and reduced flux density is a reduction in core hysteresis loss (since P_m is approximately proportional to $\hat{B}^2 f$), whilst the reduced penetration depth increases the copper loss. Thus, the overall losses remain approximately constant at the increased frequency.

Furthermore, since A16 material exhibits minimum hysteresis loss at 70°C, an increase in the ambient temperature has the effect of a slight decrease in core loss, and an increase in copper loss due to the increased resistivity of copper. There are also second-order temperature effects: an increase in eddy current core loss due to reduced ferrite resistivity, and a decrease in copper loss due to increased penetration depth. The balancing tendency of the various effects explains the minimal overall effect of an increased ambient temperature, as shown in Table 2.

The techniques described in this article have led to the production of a range of ferrite transformer cores designed specifically for application in switched-mode power supplies, and capable of meeting stringent operational and worst-case requirements. Transformer design data for each of the cores are given in the Appendix, together with optimised winding designs.

ACKNOWLEDGEMENTS

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REFERENCES

1. SNELLING, E.C., 'Soft ferrites, properties and applications', Iliffe, 1969, p.312, Eq.9.27.
2. *ibid.*, p.299, Fig.91.
3. DOWELL, P.L., 'Effects of eddy currents in transformer windings', **Proc. Instn. Elect. Engrs.**, 113, 1387 (1966).

The Appendix appears on pages 178 to 181.

For designers requiring more information on FX3700 series cores and on transformer design, a publication titled 'FX3700 series of transformer cores and coil formers for switched-mode power supplies' TP1450/1 is available on request.

APPENDIX

Transformer Design Data and Winding Designs

This Appendix gives essential design data and optimised winding designs for each core in the FX3700 series operating in a switched-mode power supply with a push-pull circuit, supplying 5V d.c. at the rated power output.

Parameter values are given for information; they may not form part of the product specification or data, and may be updated in the light of continuous development.

		FX3720	FX3730	FX3740	FX3750	
Core details (per pair of cores, assuming nominal dimensions)						
Core factor (as defined by IEC publication 205)	C_1	0.880	0.705	0.562	0.498	mm^{-1}
Total ferrite volume	V_f	7780	12600	24300	55600	mm^3
Centre pole volume	V_{cp}	1740	2950	4480	9600	mm^3
Back and leg volume	V_b	6040	9650	19820	46000	mm^3
Centre pole area	A_{cp}	71.0	106.0	141.0	211.0	mm^2
Back and leg area	A_b	96.0	130.0	222.0	386.0	mm^2
Total surface area of fully wound core	A_c	4350	5900	9100	17000	mm^2
Mean turn length	ℓ_w	50.0	60.0	73.0	95.0	mm
Transformer details						
Output current	I_2	10	20	40	100	A
Power output at rated current	P_{out}	75	150	300	750	W
Minimum secondary voltage	V_2 min	7.5	7.5	7.5	7.5	V
Minimum primary voltage	V_1 min	240	240	240	240	V
Turns ratio	$N_1:N_2$	32:1	32:1	32:1	32:1	
Minimum operating frequency	f	25	25	25	25	kHz
Number of secondary turns	$N_2 + N_2$	6 + 6	4 + 4	3 + 3	2 + 2	
Number of primary turns	$N_1 + N_1$	192+192	128+128	96+96	64+64	
Minimum primary inductance $L_1 = \dfrac{\mu_0\mu_a N_1^2}{C_1}$	L_1	52.6	29.2	20.6	10.3	mH
Maximum peak magnetising current (primary voltage E = 240V d.c.) $I_{pk} = Et_{on}/2L_1$	I_{pk}	46	82	117	233	mA
Maximum primary current (assuming 90% efficiency)	I_1	0.35	0.70	1.40	3.50	A
Minimum winding breadth (allowing 4.0mm creepage distance either side of winding)	b_w	13.4	16.4	20.2	33.3	mm

Optimisation of windings for minimum a.c. resistance

1) Primaries

At f = 25kHz and T = 100°C, the penetration depth of copper $\Delta = 0.48$mm.

For minimum leakage inductance, the primary windings are bifilar wound, an approximate layer factor F_ℓ for each winding being 0.4.

		FX3720	FX3730	FX3740	FX3750	
Layer optimisation factor	$b_w F_\ell^{3/2}/N_1\Delta$	0.036	0.067	0.110	0.54*	
Number of layers per winding portion	p	10	7	6	2*	
Number of turns per layer $N_\ell = 2N_1/p$	N_ℓ	39	37	32	32	
Preferred conductor:						
overall diameter	d_o	0.301	0.414	0.569	0.990	mm
copper diameter	d	0.250	0.355	0.500	0.900	mm
resistance	R	0.351	0.174	0.0878	0.0271	Ωm^{-1}
Layer factor of equivalent square conductor $F_\ell = N_\ell \times 0.886 \times d/2b_w$	F_ℓ	0.32	0.36	0.35	0.38	
Using Dowell's optimisation (Ref.3), factor $0.886 \times d\sqrt{F_\ell}/\Delta$		0.26	0.39	0.54	1.02	
A.C./D.C. resistance factor	F_R	1.04	1.15	1.35	1.5	
Primary a.c. resistance at 100°C $R_1(a.c.) = 1.3 \times F_R N_1 \ell_w R$	R_1 (a.c.)	4.56	2.00	1.08	0.32	Ω
Maximum primary copper loss	$I_1^2 R_1$ (a.c.)	0.56	0.98	2.12	3.9	W

*To minimise copper loss the bifilar primaries of this transformer were split into two portions, one above and one below the secondary windings.

2) Secondaries

Because of the large copper losses associated with heavy-current windings, strip conductors were considered necessary for the three larger transformers, together with winding sectionalisation on the unit employing FX3750 cores. Since the a.c. resistance of a strip winding of given breadth and length is determined by penetration depth, the strip thickness for the transformer utilising FX3740 and FX3750 cores was chosen to be that which achieved the optimum value of 1.5 for the a.c./d.c. resistance factor F_R. For the transformer utilising FX3730 cores, acceptable copper losses were obtained with strip of thickness less than the penetration depth. Hence $F_R = 1$ and the minimum winding height available determined the maximum strip thickness. The FX3720 transformer has a conventional single-layer secondary winding comprising circular cross-section conductors, bifilar wound.

Width of strip conductor	b	–	16.0	20.0	32.0	mm
Layer factor $F_\ell = b/b_w$	F_ℓ	–	0.97	0.97	0.96	
Number of layers per winding portion	p	–	4	3	1	
Value of $h\sqrt{F_\ell}/\Delta$ giving $F_R = 1.5$		–	–	0.83	1.6	

		FX3720	FX3730	FX3740	FX3750	
Strip thickness	h	–	0.15	0.40	0.80	mm
A.C./D.C. resistance factor	F_R	–	1.0	1.5	1.5	
Secondary a.c. resistance at 100°C $R_2(a.c.) = 1.3 \times F_R N_2 \ell_w \rho_c/bh$ where ρ_c = resistivity at 20°C	$R_2(a.c.)$	–	22.0×10^{-4}	9.0×10^{-4}	2.4×10^{-4}	Ω
Maximum secondary copper loss	$I_2{}^2 R_2(a.c.)$	–	0.88	1.44	2.40	W
For single layer, number of turns	$2N_2$	12				
Preferred conductor:						
overall diameter	d_o	1.093				mm
copper diameter	d	1.000				mm
resistance	R	0.0219				Ωm^{-1}
Layer factor	F_ℓ	0.38				
Factor $0.886 \times d \sqrt{F_\ell}/\Delta$		1.14				
A.C./D.C. resistance factor	F_R	1.18				
$R_2(a.c.) = 1.3 \times F_R N_2 \ell_w R$	$R_2(a.c.)$	0.01				Ω
Maximum secondary copper loss	$I_2{}^2 R_2(a.c.)$	1.00				W

Core losses

These are calculated for a pair of cores of nominal size, assuming operation at 100°C and material having the maximum limit hysteresis loss at this temperature. The core is considered in two sections having areas and volumes A_{cp}, A_b and V_{cp}, V_b respectively.

For any section, the maximum flux density

$\hat{B} = E/4 N_1 A f$

where E = 240V,

the transistor 'on' time is a maximum,

N_1 is the number of primary turns,

A is the area of the section considered, and

f = 25kHz.

	FX3720	FX3730	FX3740	FX3750	
$\hat{B}$ in centre pole	177	177	177	177	mT
P_m max at f = 25kHz (from Fig.1)	135	135	135	135	$\mu W\, mm^{-3}$
Centre pole hysteresis loss $V_{cp} P_m \times 10^{-6}$	0.24	0.40	0.61	1.30	W
$\hat{B}$ in back and legs	130	144	113	97	mT
P_m max at f = 25kHz	60	80	40	26	$\mu W\, mm^{-3}$
Hysteresis loss in back and legs $V_b P_m \times 10^{-6}$	0.36	0.77	0.80	1.20	W
Total core hysteresis loss	0.60	1.17	1.41	2.50	W

	FX3720	FX3730	FX3740	FX3750	
Similarly, eddy current core loss has been calculated from $\frac{(\pi B f D)^2 V}{16\rho}$	0.01	0.05	0.09	0.29	W

where D and V are the equivalent diameter and volume respectively of the core section considered, and ρ is the material resistivity = 0.4Ωm at 100°C.

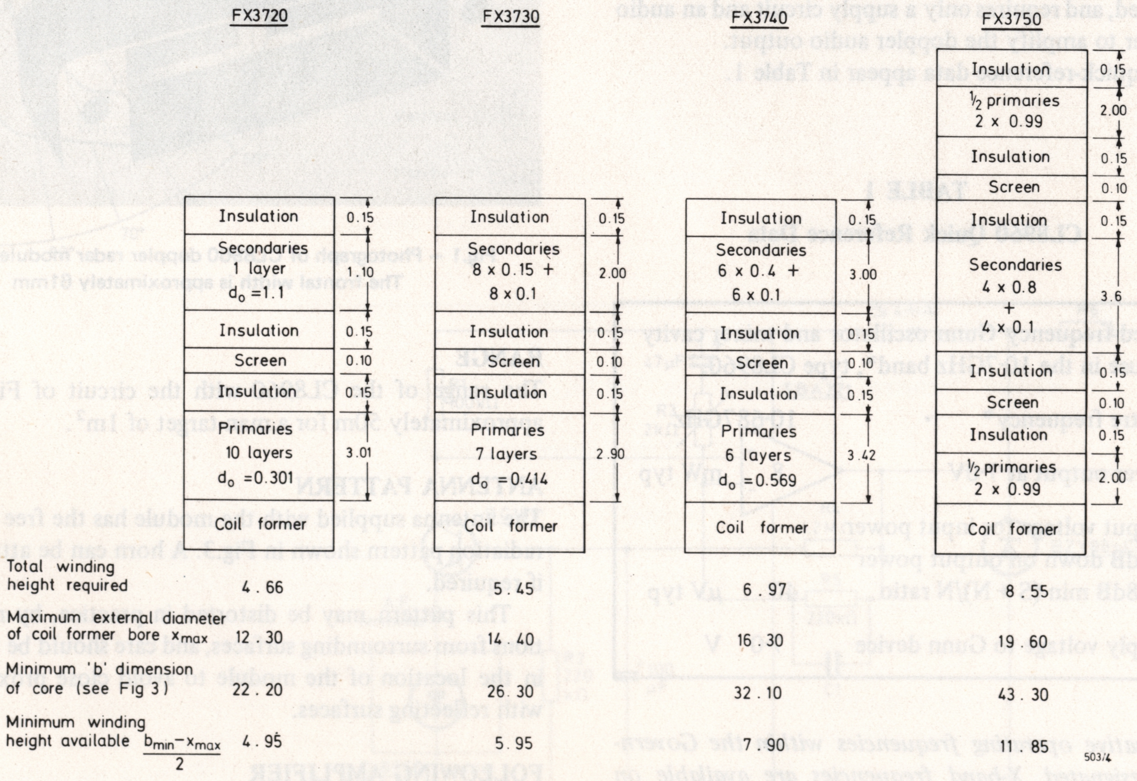
	FX3720	FX3730	FX3740	FX3750	
Total core losses	0.61	1.22	1.50	2.79	W
Total transformer loss (core and copper)	2.17	3.08	5.06	9.09	W
Specific dissipation	498	522	556	534	$\mu W\, mm^{-2}$

It can be seen from Ref.2 that for values of specific dissipation within the range from 500 to 560μWmm^{-2}, the predicted temperature rise lies between 38 and 42degC (assuming free air convection and radiation from a body of uniform surface temperature). In practice it is found that the highest temperature occurs at the region where the core centre pole emerges from the coil former. The temperatures at the core extremities are appreciably lower.

Winding construction

An approximate winding construction is given in Fig.4, based on the following assumptions:

1) 0.1mm copper screens (overlapped but not shorted) between windings;
2) insulation capable of withstanding a 2kV flash-test, that is, a minimum of 0.1mm Makrofol between windings and screens;
3) primary conductors 'square' wound and with grade II insulation;
4) 0.1mm insulation between secondary strip conductors.


FX3720
Insulation 0.15
Secondaries 1 layer d_o =1.1 1.10
Insulation 0.15
Screen 0.10
Insulation 0.15
Primaries 10 layers d_o =0.301 3.01
Coil former
FX3730
Insulation 0.15
Secondaries 8 x 0.15 + 8 x 0.1 2.00
Insulation 0.15
Screen 0.10
Insulation 0.15
Primaries 7 layers d_o =0.414 2.90
Coil former
FX3740
Insulation 0.15
Secondaries 6 x 0.4 + 6 x 0.1 3.00
Insulation 0.15
Screen 0.10
Insulation 0.15
Primaries 6 layers d_o =0.569 3.42
Coil former
FX3750
Insulation 0.15
½ primaries 2 x 0.99 2.00
Insulation 0.15
Screen 0.10
Insulation 0.15
Secondaries 4 x 0.8 + 4 x 0.1 3.6
Insulation 0.15
Screen 0.10
Insulation 0.15
½ primaries 2 x 0.99 2.00
Coil former
503/4

	FX3720	FX3730	FX3740	FX3750
Total winding height required	4.66	5.45	6.97	8.55
Maximum external diameter of coil former bore x_{max}	12.30	14.40	16.30	19.60
Minimum 'b' dimension of core (see Fig 3)	22.20	26.30	32.10	43.30
Minimum winding height available $\frac{b_{min} - x_{max}}{2}$	4.95	5.95	7.90	11.85

Fig.4 – Optimised winding designs for transformers using cores FX3720, FX3730, FX3740, and FX3750
All dimensions in millimetres (not to scale)

Product Information:

CL8960 X-band doppler radar module

The X-band doppler module CL8960 shown in Fig.1 is a device designed specifically for detecting movement of a remote target by detecting doppler-shift in microwave radiation reflected from the target. The CL8960 contains a Gunn oscillator, which produces the energy to be radiated, and a mixer cavity which mixes the reflected energy with a sample of the oscillator signal. The unit is self-contained, and requires only a supply circuit and an audio amplifier to amplify the doppler audio output.

The quick-reference data appear in Table 1.

TABLE 1

CL8960 Quick Reference Data

Fixed-frequency Gunn oscillator and mixer cavity for use in the 10·7GHz band*, type CL8960.		
Centre frequency*	10·687GHz	
Power output at 7·0V	8	mW typ
Output voltage for input power 100dB down on output power at 18dB min (S + N)/N ratio	40	µV typ
Supply voltage to Gunn device	7·0	V

**Alternative operating frequencies within the Government-designated X-band frequencies are available on request. Alternative antenna systems can be made available.*

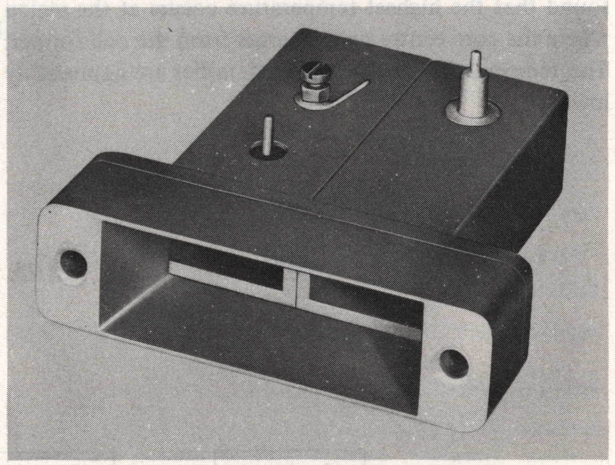


Fig.1 – Photograph of CL8960 doppler radar module. The frontal width is approximately 61mm

RANGE

The range of the CL8960 with the circuit of Fig.2 is approximately 50m for a man-target of $1m^2$.

ANTENNA PATTERN

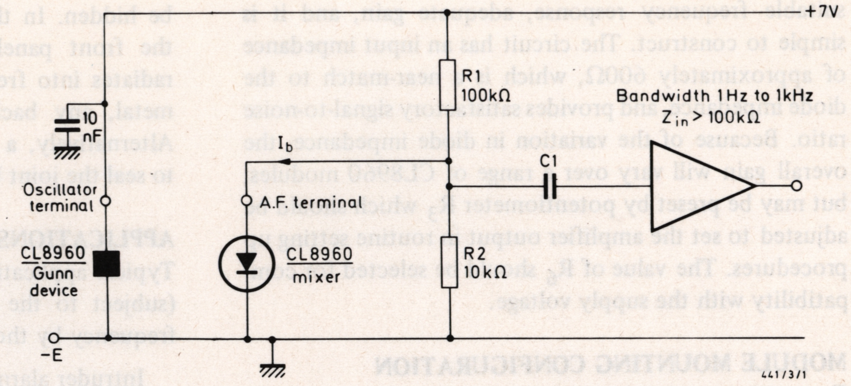
The antenna supplied with the module has the free space radiation pattern shown in Fig.3. A horn can be attached if required.

This pattern may be distorted in practice, by reflections from surrounding surfaces, and care should be taken in the location of the module to avoid close proximity with reflecting surfaces.

FOLLOWING AMPLIFIER

A circuit design shown in Fig.4 will provide the optimum mixer d.c. bias; it has low noise characteristics, a

Fig.2 – Circuit used for obtaining CL8960 performance figures


+7V
10 nF
Oscillator terminal
CL8960 Gunn device
-E
R1 100kΩ
I_b
A.F. terminal
CL8960 mixer
R2 10kΩ
C1
Bandwidth 1Hz to 1kHz
Z_{in} > 100kΩ
441/3/1

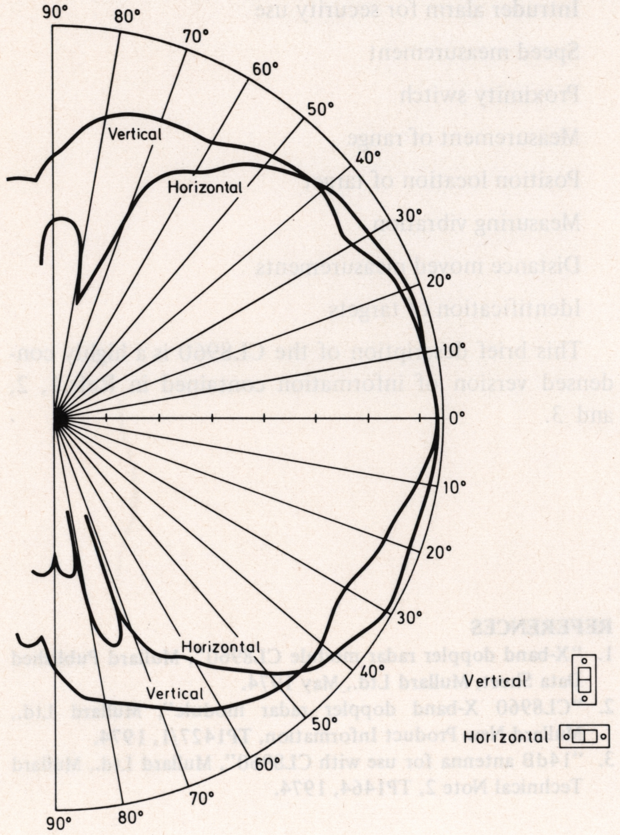


Fig.3 – Polar diagram for CL8960 without additional horn

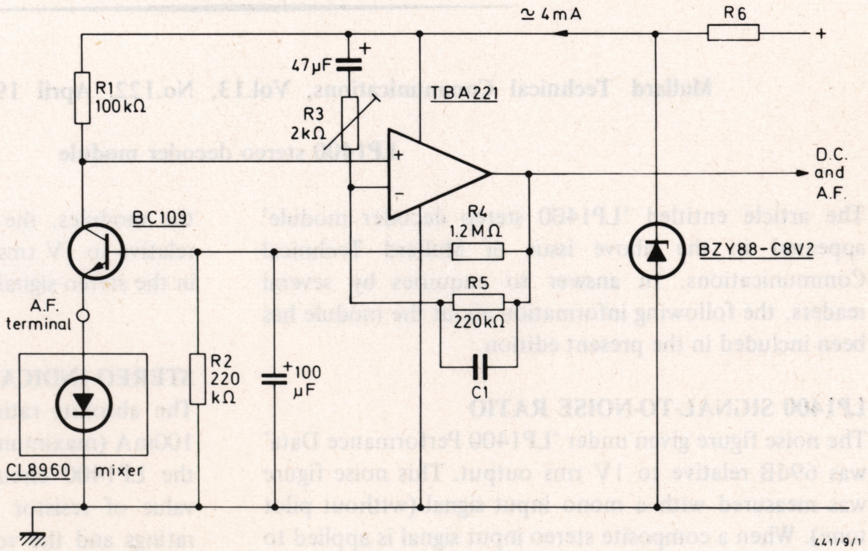

≃4mA
R6
+
47µF
TBA221
R1 100kΩ
R3 2kΩ
D.C. and A.F.
BC109
R4 1.2MΩ
BZY88-C8V2
R5 220kΩ
C1
A.F. terminal
R2 220 kΩ
100 µF
CL8960 mixer
441/9/1

Fig.4 – Low impedance amplifier for use with CL8960

suitable frequency response, adequate gain, and it is simple to construct. The circuit has an input impedance of approximately 600Ω, which is a near-match to the diode impedance, and provides satisfactory signal-to-noise ratio. Because of the variation in diode impedance, the overall gain will vary over a range of CL8960 modules, but may be preset by potentiometer R_3 which should be adjusted to set the amplifier output in routine setting up procedures. The value of R_6 should be selected for compatibility with the supply voltage.

MODULE MOUNTING CONFIGURATION

For optimum signal-to-noise ratio, it is recommended that the module and antenna are mounted using M4 screws, to a 1·6mm thick metal plate with an aperture. Fig.5 shows the CL8960 mounted with a thin plastic sheet over the aperture to indicate how the device may be hidden. In this configuration, the metal plate forms the front panel of the equipment, and the antenna radiates into free space. If the equipment-housing is all metal, any back radiation will be totally contained. Alternatively, a metal-based adhesive tape may be used to seal the joint between antenna and mounting plate.

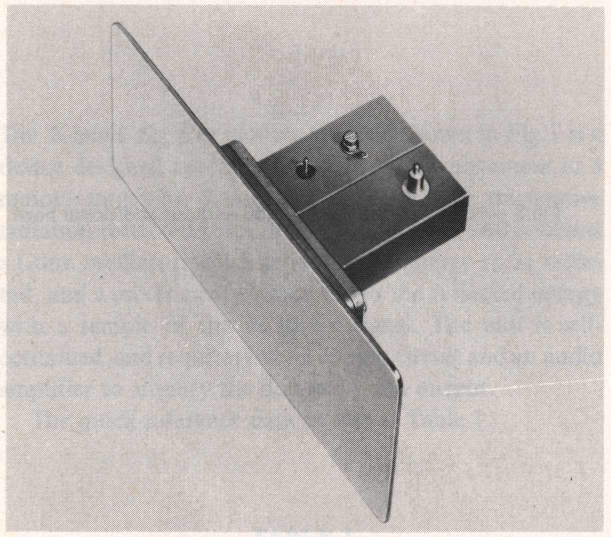


Fig.5 — Mounted CL8960 module

APPLICATIONS PROPOSALS

Typical applications for which systems may be designed (subject to the approval of the 10·687GHz operating frequency by the controlling authority) are listed below.

Intruder alarm for security use
Speed measurement
Proximity switch
Measurement of range
Position location of target
Measuring vibration
Distance moved measurements
Identification of targets

This brief description of the CL8960 is a highly condensed version of information contained in Refs.1, 2, and 3.

REFERENCES

1. "X-band doppler radar module CL8960", Mullard Published Data Sheet, Mullard Ltd., May 1974.
2. "CL8960 X-band doppler radar module", Mullard Ltd., Mullard New Product Information, TP1427/1, 1974.
3. "14dB antenna for use with CL8960", Mullard Ltd., Mullard Technical Note 2, TP1464, 1974.

Mullard Technical Communications, Vol.13, No.122, April 1974, pages 80 to 87

LP1400 stereo decoder module

The article entitled 'LP1400 stereo decoder module' appeared in the above issue of Mullard Technical Communications. In answer to enquiries by several readers, the following information about the module has been included in the present edition.

LP1400 SIGNAL-TO-NOISE RATIO

The noise figure given under 'LP1400 Performance Data' was 69dB relative to 1V rms output. This noise figure was measured with a mono input signal (without pilot tone). When a composite stereo input signal is applied to the modules, the typical signal-to-noise ratio is 45dB, relative to 1V rms output. No output filtering was used in the stereo signal-to-noise measurements.

STEREO INDICATOR LAMP

The absolute ratings for the stereo indicator lamp are 100mA (maximum surge current) at 28V maximum. In the LP1400 circuit shown in Fig.6 in the article, the value of resistor R_7 is chosen according to the lamp ratings and the voltage V_L.